700V 59mΩ SolidGaN with DESAT Protection

1. Features

- 59mΩ E-Mode GaN with Integrated Gate Clamp
- 700V Continuous, 800V Transient Voltage Rating
- Wide 10V to 24V Gate Input Voltage Range
- Adjustable Turn-On and Turn-Off Slew Rate
- Integrated Miller Clamp
- dv/dt Immunity up to 100V/ns
- Paralleling Capability
- Zero Reverse Recovery Charge
- High Frequency Operation up to 2MHz
- Short Circuit Protection with Built-In DESAT
- Input UVLO and OTP Protection
- Available in TOLT-16L Package

2. Applications

- High-Power Switch-Mode Power Supplies
- AC-DC, DC-DC, DC-AC Converters
- Half-Bridge and Full-Bridge Converters
- Data Center / AI Server PSU
- Air Conditioner, Solar Inverter, Motor Drive
- Automotive OBC & DC-DC Converter

3. Description

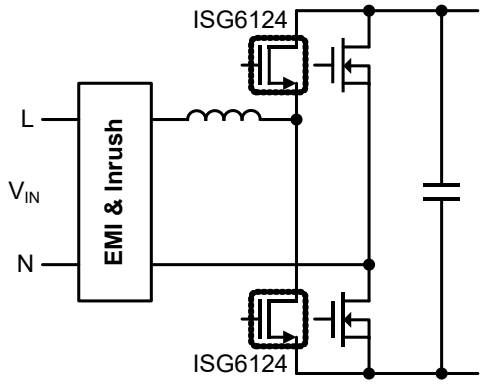
The ISG6124 SolidGaN IC seamlessly integrates a 700V E-Mode GaN FET with advanced features, setting a new standard for performance, easy-of-use, and reliability in power electronics. The integrated gate clamp, driven by an accurate LDO-based circuitry, maintains a tightly regulated driving voltage for the GaN FET within a flexible gate-input voltage range of 10V to 24V, ensuring full protection of the GaN power transistor against excessive voltage stress while maximizing GaN performance.

The ISG6124 offers users the ability to adjust the turn-on and turn-off slew rate of the GaN FET with external gate resistors, optimizing both EMI and power efficiency. Equipped with built-in protections including DESAT protection, Input UVLO, and OTP, the ISG6124 further ensures device robustness and system safety. The integrated miller clamp prevents false turn-on caused by the high dv/dt slope of the drain voltage.

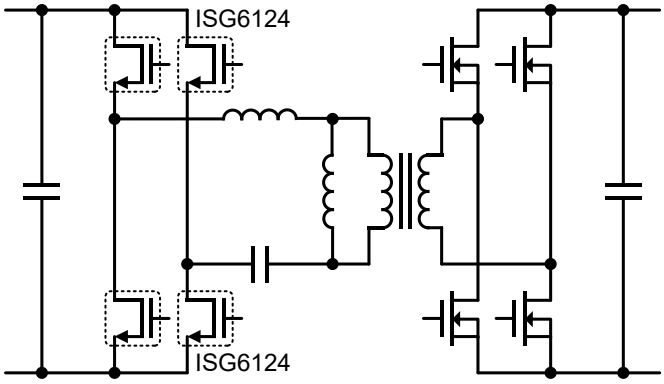
The ISG6124's high integration level with a GaN FET and robust protection, makes it suitable for a range of applications, from simple setups with low component counts to high-frequency and high-power applications.

4. Typical Application

Totem Pole PFC



LLC Resonant Converter



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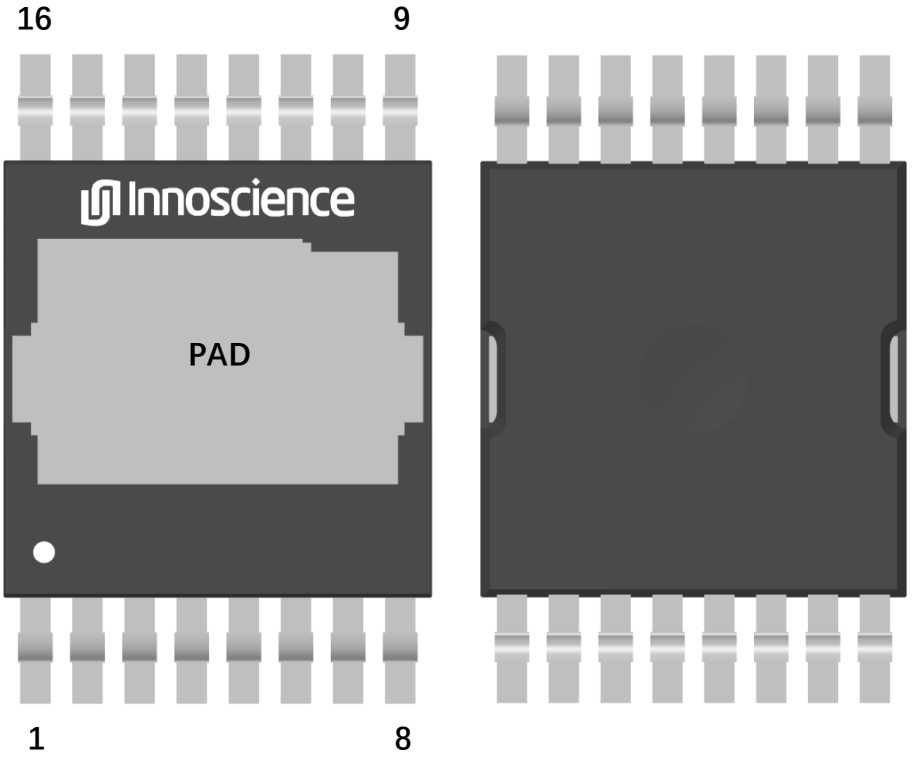
5. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2025-06-25	Final datasheet release

6. Pin Configuration and Functions



16-Lead TOLT Package – Top and Bottom View

Pin Number	Pin Name	Description
1-8	D	Drain of Power GaN FET.
11-16, PAD	S	Source of Power GaN FET.
10	K	Kelvin Source.
9	G	Gate Input. Connect to the drive output of controller or gate driver.

7. Absolute Maximum Ratings

All pins are referred to S pins, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device lifetime.

Parameter	Value	Unit
Drain Voltage, Continuous	700	V
Drain Voltage, Transient (1)	800	V
Drain Voltage, Pulsed (2)	750	V
Drain Current, Continuous (T_C = 25°C)	35	A
Drain Current, Continuous (T_C = 125°C)	22	A
Drain Current, Pulsed (10us @ T_C = 25°C)	66	A
Drain Current, Pulsed (10us @ T_C = 125°C)	33	A
Gate Input Voltage, Continuous	-0.6 to 26	V
Gate Input Voltage, Pulsed (2)	-5 to 26	V
Drain-to-Source Slew Rate – dV/dt	100	V/ns
Power Dissipation (T_C = 25°C)	260	W
Operating Junction Temperature T_J	-55 to 150	˚C
Storage Temperature	-55 to 150	˚C

(1) Intended for non-repetitive events, t_{PULSE} < 200us.

(2) Intended for repetitive events, t_{PULSE} < 100ns.

8. ESD Ratings

T_J = 25°C unless otherwise specified.

Parameter	Value	Unit
Human Body Model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
Charged Device Model (CDM), per ANSI/ESDA/JEDEC JS-002	±1000	V

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
Gate Input High Voltage	10	24	V
Gate Input Low Voltage	-0.3	0.3	V

10. Thermal Information

Symbol	Parameter	ISG6124TP	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	48.94	˚C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.48	˚C/W

According to standards defined in JESD51 and JESD51-1, thermal characteristics of the package are simulated. $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

11. Electrical Characteristics

T_J = 25°C, V_{GS} = 15V, V_{DS} = 400V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Gate Characteristics						
Gate input high threshold (3)	V_{G_HI}		4		V	Gate Rising
Gate input low threshold (3)	V_{G_LO}		3.3		V	Gate Falling
Gate quiescent current	I_{G_Q}		1.9	5.2	mA	V_{GS} = 15V, V_{DS} = 0V
Protection						
DESAT protection threshold (3)	V_{D_DESAT}		7.3		V	
DESAT blanking time (3)	t_{BLK_DESAT}		300		ns	
Gate UVLO threshold	V_{G_UVLO}	8.2	8.7	9.3	V	
Over temperature threshold (3)	T_{OTP}		160		°C	
Over temperature hysteresis (3)	T_{HYS}		20		°C	
Power GaN FET						
Drain-source leakage current	I_{DSS}		6	80	uA	V_{DS} = 700V, V_{GS} = 0V
Drain-source resistance	$R_{DS(ON)}$		59	77	mΩ	V_{GS} = 15V, I_{DS} = 8A
Drain-source resistance (3)	$R_{DS(ON)}$		130		mΩ	V_{GS} = 15V, I_{DS} = 8A, T_J = 150°C
Source-drain reverse voltage	V_{SD}		2.8		V	V_{GS} = 0V, I_{SD} = 4A
Total gate charge (3)	Q_G		7.4		nC	
Output charge (3)	Q_{OSS}		80		nC	V_{DS} = 400V, V_{GS} = 0V
Reverse recovery charge (3)	Q_{RR}		0		nC	
Input capacitance (3)	C_{ISS}		269		pF	
Output capacitance (3)	C_{OSS}		98		pF	V_{DS} = 400V, V_{GS} = 0V
Effective output capacitance, energy related (3)	$C_{O(er)}$		146		pF	V_{DS} = 400V, V_{GS} = 0V
Effective output capacitance, time related (3)	$C_{O(tr)}$		200		pF	V_{DS} = 400V, V_{GS} = 0V

12. Switching Characteristics

T_J = 25°C, V_{GS} = 15V, V_{DS} = 400V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Minimum input pulse width that changes the output (3)	t_{GH_PW}		20		ns	
Turn-on propagation delay (3)	t_{ON_PD}		35		ns	
Turn-off propagation delay (3)	t_{OFF_PD}		20		ns	
Minimum on time (3)			30		ns	
Rise time (3)	t_r		10		ns	
Fall time (3)	t_f		10		ns	

(3) Not 100% tested and guaranteed by design.

13. Typical Characteristics

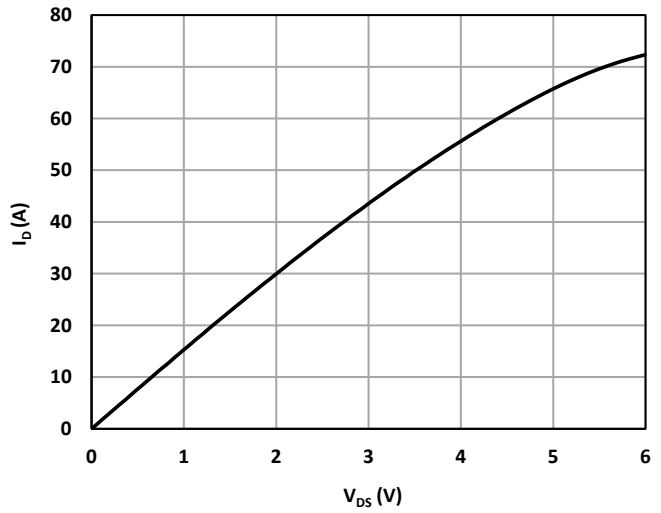


Figure 1. Drain Current vs. Drain-to-Source Voltage, T_J=25°C

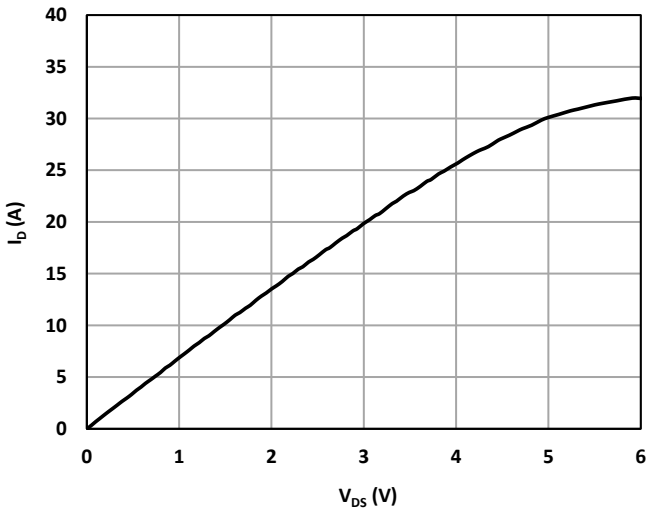


Figure 2. Drain Current vs. Drain-to-Source Voltage, T_J=150°C

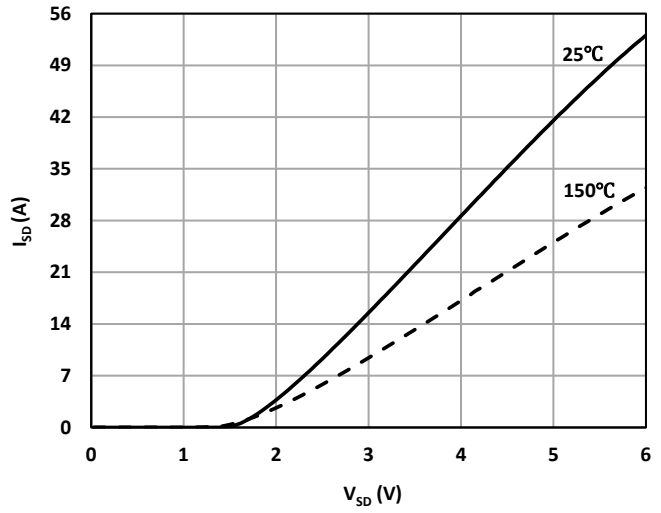


Figure 3. Source-Drain Reverse Conduction Voltage, T_J=25°C

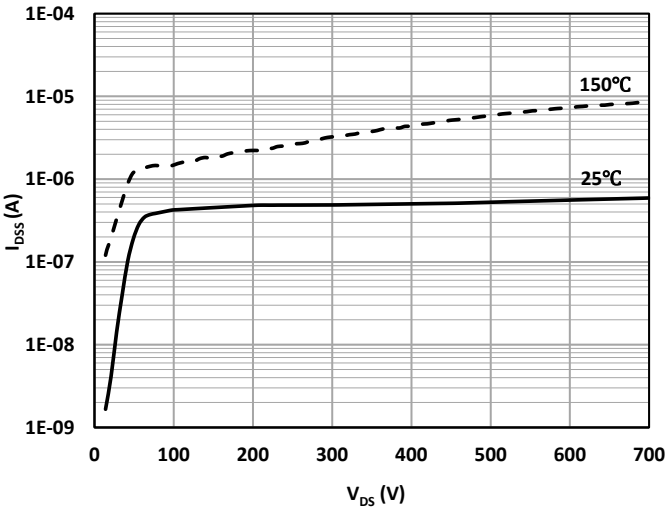


Figure 4. Drain Leakage Current vs Drain Voltage

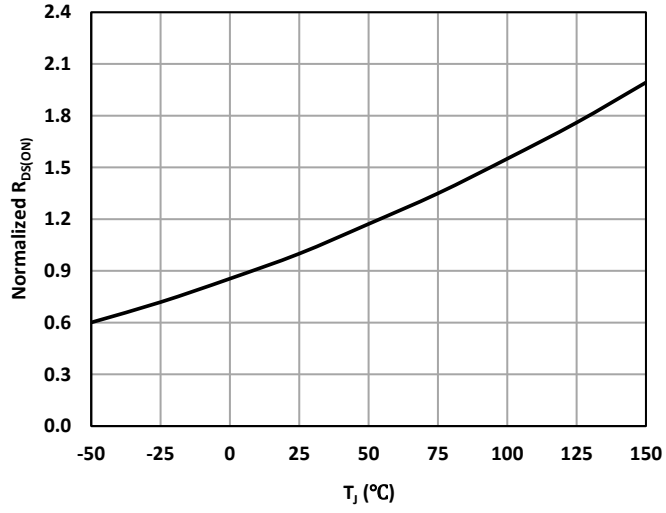


Figure 5. Normalized $R_{DS(ON)}$ vs Temperature

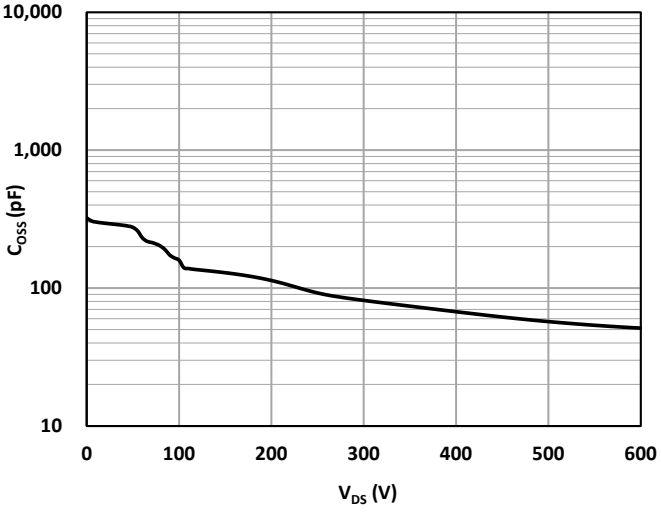


Figure 6. Output Capacitance vs Drain Voltage

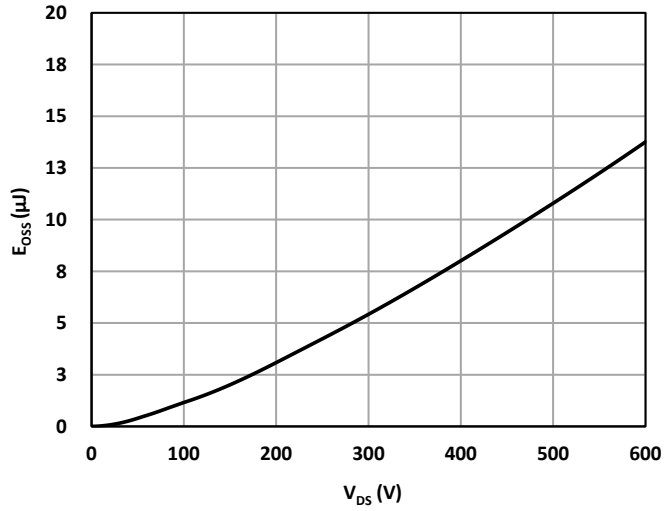


Figure 7. Output Capacitance Stored Energy vs Drain Voltage

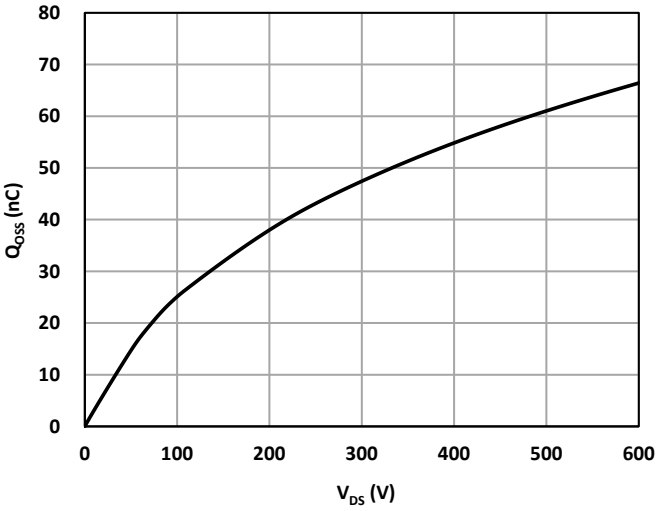


Figure 8. Output Charges vs Drain Voltage

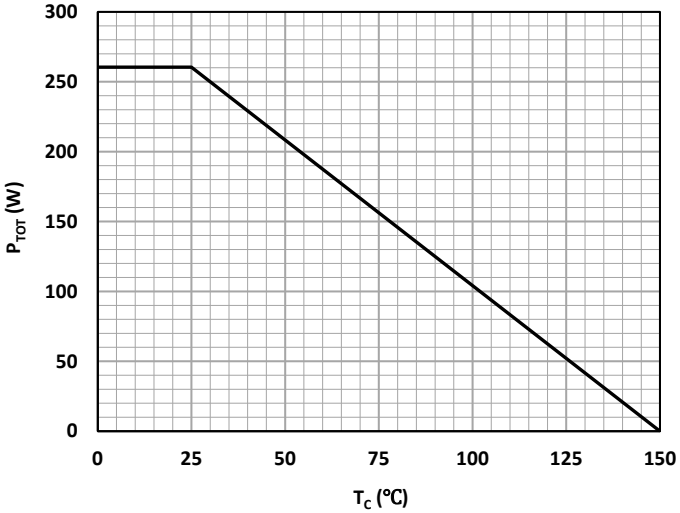


Figure 9. Power Dissipation

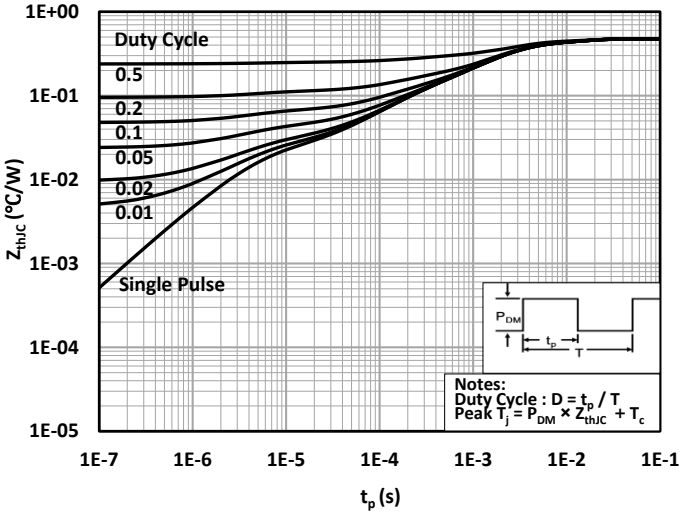


Figure 10. Max. Transient Thermal Impedance

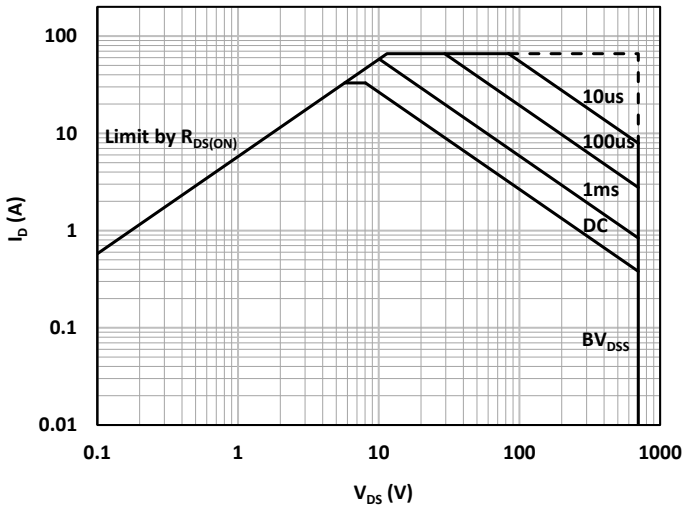


Figure 11. Safe Operating Area, T_J=25°C

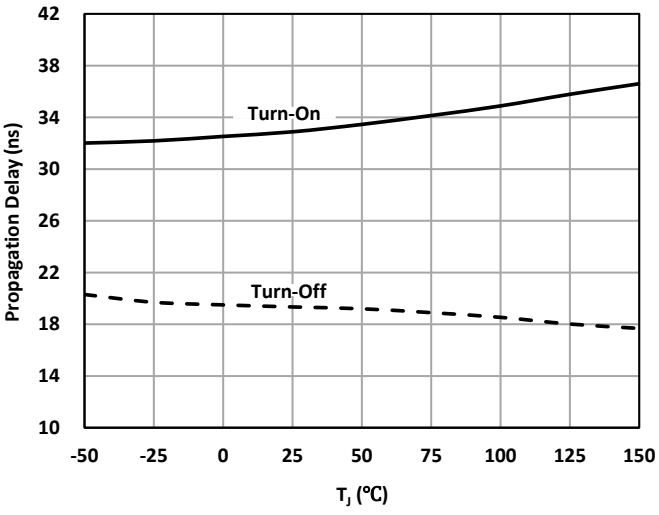


Figure 12. Turn-On/Off Propagation Delay vs Temperature

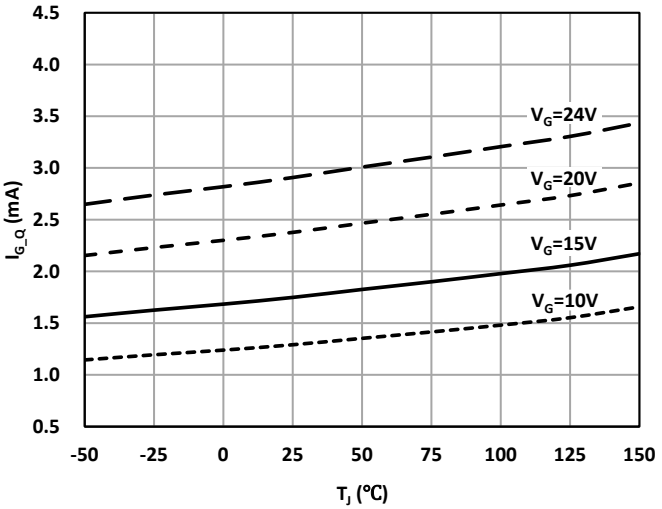


Figure 13. Gate Quiescent Current vs Temperature

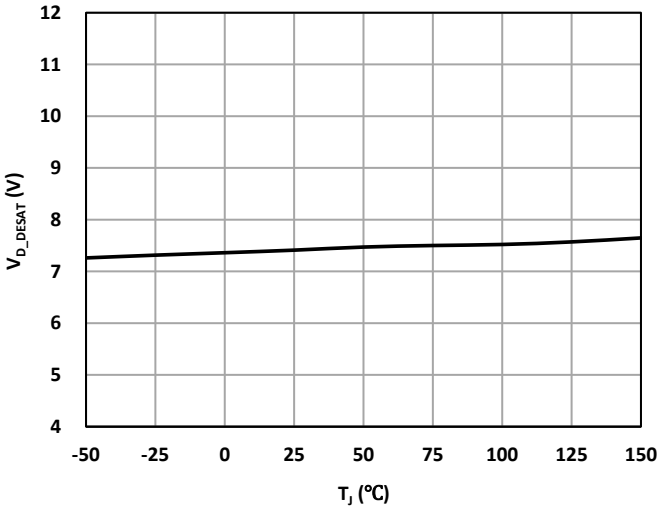


Figure 14. DESAT Threshold Voltage vs Temperature

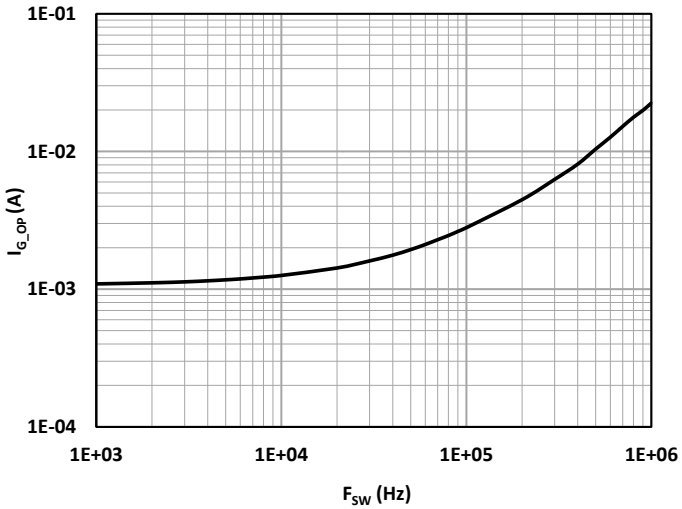


Figure 15. Gate Operating Current vs Switching Frequency

14. Block Diagram

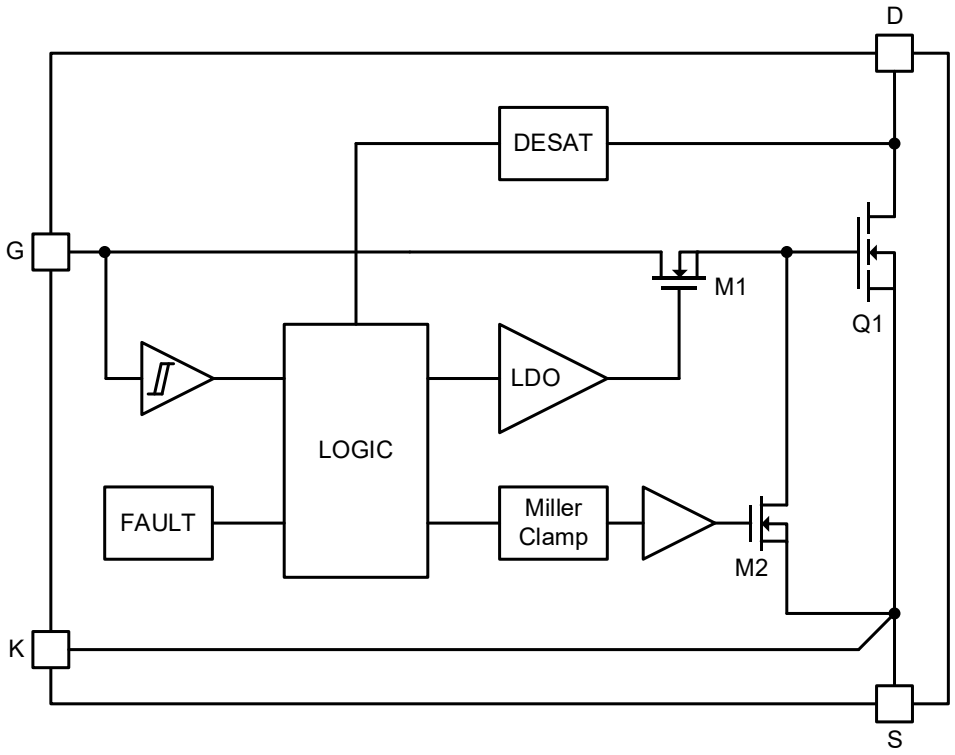


Figure 16. Functional Block Diagram

15. Function Description

The ISG6124 is a 700V SolidGaN IC integrating a high-performance enhancement-mode GaN FET with advanced features, offering the most reliable, efficient, and easy-to-use GaN power device.

The ISG6124 features a gate clamp to provide a wide G input voltage range of 10V to 24V. With an accurate LDO-based circuitry, the gate voltage is tightly regulated to protect the GaN FET from excessive voltage stress while maximizing the performance. The ISG6124 allows adjusting both turn-on and turn-off slew rate of the GaN FET by adding external gate resistors, optimizing both EMI and efficiency.

Rich fault protection is provided including de-saturation (DESAT) protection, input undervoltage lockout (UVLO), and over temperature protection (OTP). The ISG6124 integrates a miller clamp with a strong pull-down strength at the gate, preventing high dv/dt induced false turn-on of the GaN FET. All the features are provided without requiring a sustainable supply voltage for internal supply.

Highly integrated with a GaN FET and robust protection in a TOLT-16L package, the ISG6124 offers simple setups with low component counts and drives next-generation high-frequency and high-power applications.

Input and Output

The ISG6124 has an input pin, G, to control the integrated GaN FET. When the input G voltage exceeds the input high threshold (4.0V typical), the ISG6124 propagates the input signal to the gate of GaN FET, turning the GaN FET on and shorting the drain, D, to the source, S, with a resistance of 59mΩ (typical). When the input G voltage falls below the input low threshold (3.3V typical), the ISG6124 blocks the input-signal propagation and pulls down the gate of GaN FET

to S, turning the GaN FET off and opening the output of D. Figure 17 illustrates the timing diagram of the input and output with the gate-to-source voltage of the GaN FET, V_{GS}. The ISG6124 features a 10ns (typical) input deglitch filter for turn-on to remove unwanted pulses from the G input. A narrow input pulse exceeding this deglitch delay time will be extended to a minimum output pulse of 40ns (typical).

The ISG6124 provides a wide G input voltage range of 10V to 24V for the maximum flexibility. This is achieved by integrating internal gate clamp driven by an accurate LDO-based circuitry, ensuring a tightly regulated gate voltage to protect the GaN FET from excessive voltage stress while maximizing the performance.

The internal circuitry of the ISG6124 is powered from the G input, eliminating the need for a sustainable supply voltage from an external power source.

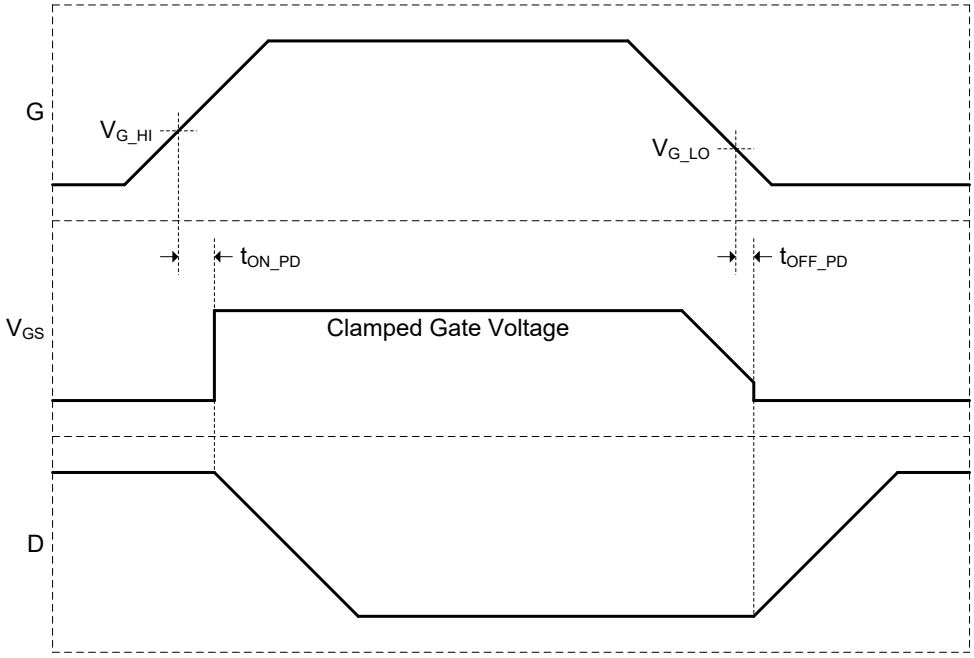


Figure 17. Timing Diagram of Input and Output

Adjustable Turn-On and Turn-Off Slew Rate

The ISG6124 supports users the ability to adjust both turn-on and turn-off slew rate of the GaN FET independently. This is achieved by adding external gate resistors and diode between the driver output and G pin of ISG6124 as shown in Figure 18, targeting optimization of efficiency, reliability, and EMI performance.

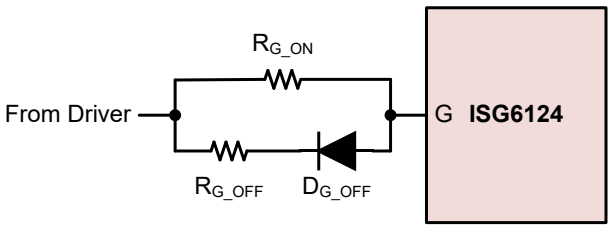


Figure 18. Configuration of Adjustable Turn-On and Turn-Off Slew Rate

Integrated Miller Clamp

GaN FETs can switch much faster than traditional silicon based MOSFETs, resulting in higher dv/dt slope of the drain voltage. The ISG6124 integrates a miller clamp with a strong pull-down strength of 0.5Ω (typical) at gate to provide a

robust low impedance path necessary for eliminating high dv/dt induced gate turn-on. This feature allows to remove negative power supply for gate drivers in a conventional design.

DESAT Protection

The ISG6124 provides cycle-by-cycle DESAT protection by monitoring the drain-source voltage, V_{DS}, to protect the GaN FET from potential damage in the desaturation region. As illustrated in the timing diagram of Figure 19, when the V_{DS} exceeds the DESAT protection threshold (7.3V typical), the GaN FET is turned off. The GaN FET will be turned on again at the next rising edge of G signal. The blanking time of 300ns (typical) is added to prevent false triggering during the GaN FET turn-on.

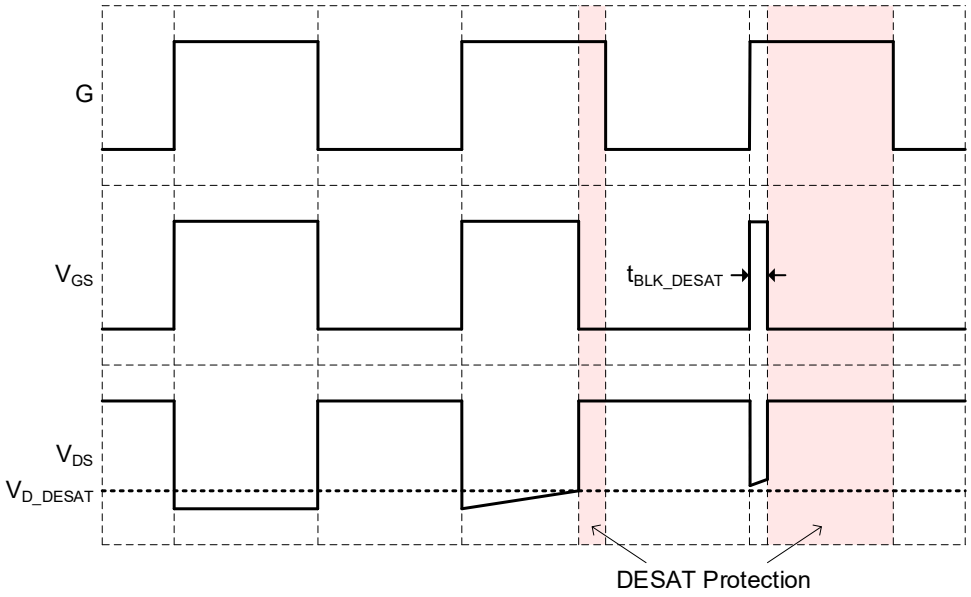


Figure 19. Timing Diagram of DESAT Protection

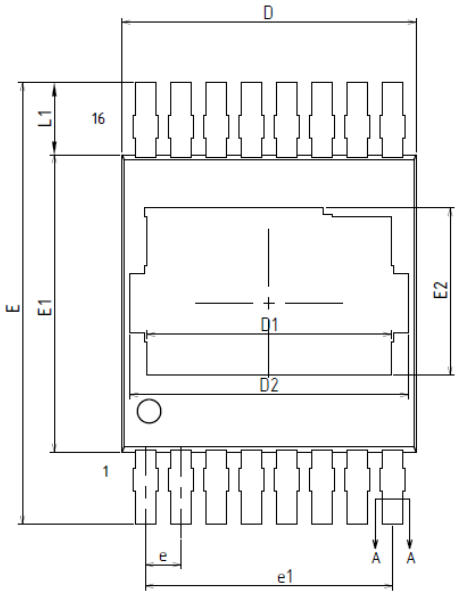
Input UVLO Protection

The ISG6124 features a cycle-by-cycle UVLO protection for G input, ensuring the operation under the robust conditions of devices. When the G voltage is below its UVLO threshold (8.7V typical), the ISG6124 enters UVLO mode and turns off the GaN FET. The GaN FET will be turned on again at the next rising edge of G signal.

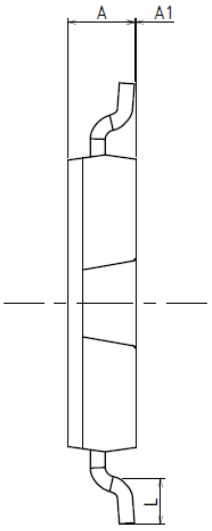
Over Temperature Protection (OTP)

The ISG6124 features OTP protection. If the internal junction temperature, T_j, exceeds 160°C (typical), the G input is ignored and the GaN FET is turned off. When the temperature recovers to below 140°C (typical), the ISG6124 will resume normal operation.

16. Package Information

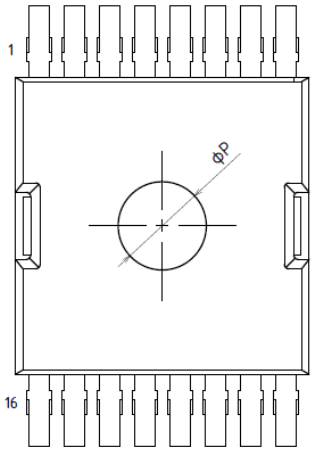


top view

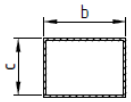


side view

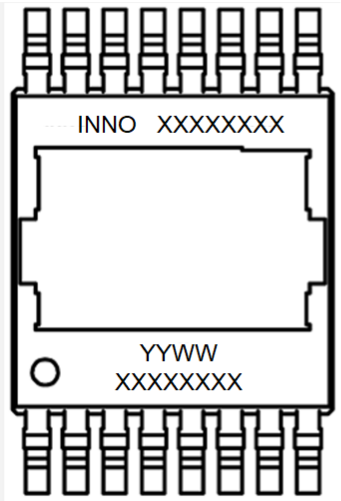
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.20	2.30	2.40
A1	0.01	0.08	0.16
b	0.60	0.70	0.85
c	0.40	0.50	0.65
D	9.70	9.90	10.10
D1	8.10	8.30	8.50
D2	9.46REF		
E	14.80	15.00	15.20
E1	9.90	10.10	10.30
E2	5.47	5.67	5.87
e	1.20BSC		
e1	8.40BSC		
L	1.30	1.50	1.70
L1	2. 45REF		
φP	2.90	3.00	3.10



Bottow view

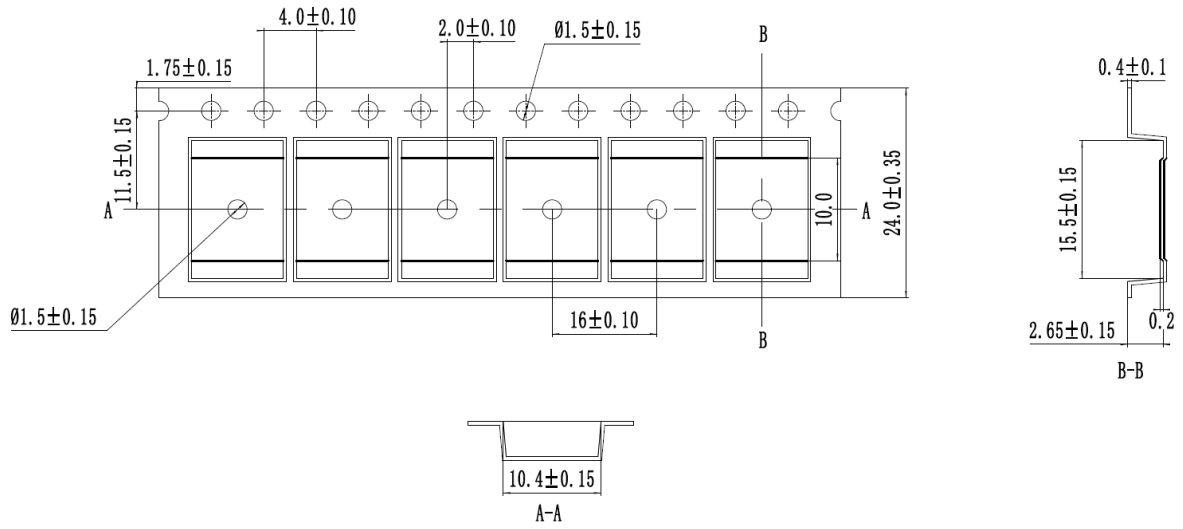


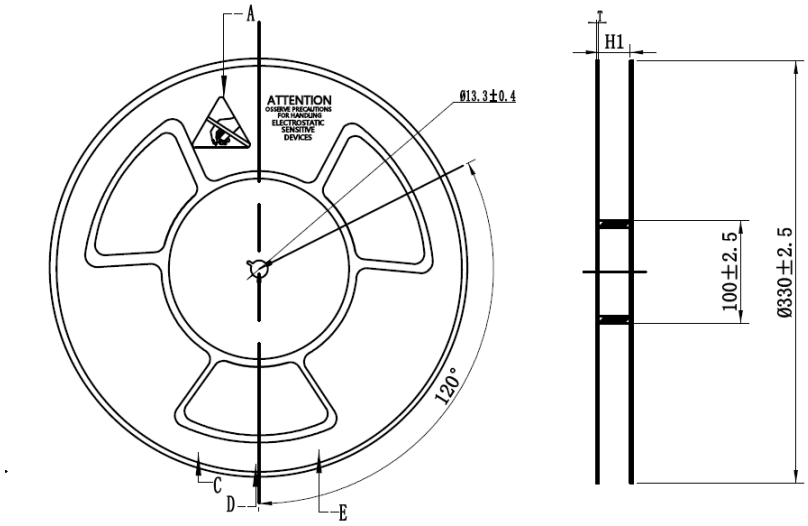
setion A-A



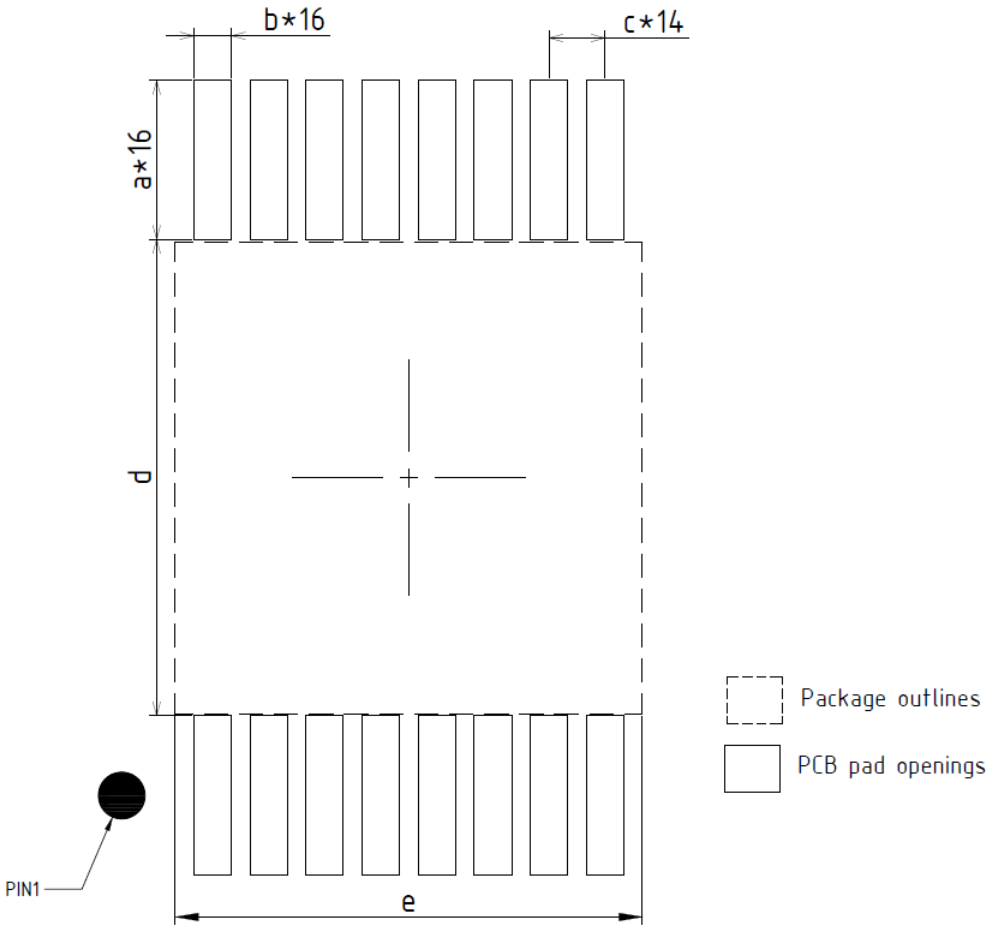
ROW	Description	Example
Row1	Company Name	INNO
Row1	Product Code (In short)	XXXXXXXX
Row2	Date Code	YYWW
Row3	ASSY lot No.	XXXXXXXX

17. Tape and Reel Information





18. Recommended Land Pattern



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	3.40	d	10.20
b	0.80	e	10.00
c	1.20		

Notes:
(1)All dimension are in millimeters.
(2)Drawing is not to scale.

19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
ISG6124TP	TOLT-16L	6124TP	MSL3	13" 2500PCS/reel

Important Notice

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