

100V Half-Bridge SolidGaN™ with Integrated Gate Driver

1. Features

- 3.1mΩ(HS)/2.7mΩ(LS) Half-Bridge GaN FETs with Gate Driver
- 80V Continuous, 100V Transient Voltage Rating
- Capable of up to 5MHz Switching
- Independent High-Side and Low-Side PWM Inputs
- High-Side and Low-Side Driver Interlocking
- Internal Strong and Smart Bootstrap Switch
- Adaptive Shoot-Through Protection
- Fast Propagation Delay (20ns Typical)
- Excellent Delay Matching (1ns Typical)
- Built-In UVLO, OVLO, OTP Protections
- 35μA Low VCC Quiescent Current
- Integrated VCC/BST capacitors
- High dv/dt Immunity up to 50V/ns
- Adjustable Turn-on Speeds
- Optimized for Easy and Low-EMI PCB Layout
- En-LGA 6.5mmx6.5mm with Top Side Cooling

2. Applications

- Half Bridge, Full Bridge, SR in LLC Converters
- High Frequency Buck and Boost Converter
- Datacenter and Automotive Power Supply
- Class-D Audio, Motor Drive Applications

3. Description

The ISG3208 is a 100V, 45A, half-bridge SolidGaN in a compact 6.5mm x 6.5mm LGA package. Included in the package are two high-performance GaN FETs, drivers, and driver supply capacitors, offering the industry's most compact and efficient GaN power solution.

The ISG3208 provides two logic inputs for controlling the high-side and low-side GaN FETs for maximum flexibility. The split driver outputs allow for independent adjustment of turn-on and turn-off strengths, optimizing both EMI and efficiency.

The ISG3208 features input interlocking with internal adaptive shoot-through protection circuit, ensuring no simultaneous output conduction even at near zero dead time. Comprehensive fault protection is built into the ISG3208, including active bootstrap (BST) voltage control to prevent overcharge and ensure stable gate drive voltage, independent UVLO and OVLO for both VCC and BST, and over temperature protection.

With fast propagation delay, excellent delay matching, superior dv/dt immunity, and ultra-low in-package parasitic inductance loop, the ISG3208 enables designers to achieve substantial improvement in power density and efficiency.

4. Typical Application

36V – 80V Input, 12V Output, and 300W Buck Converter

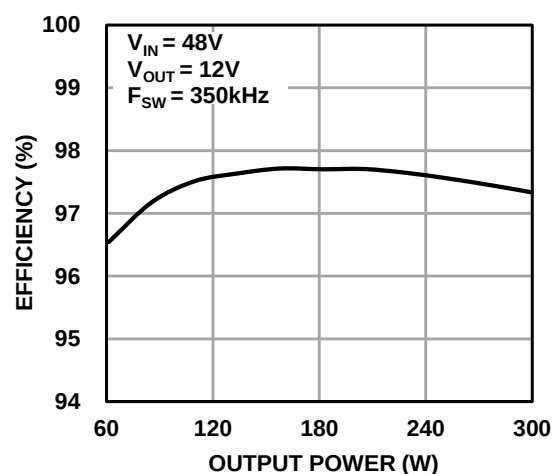
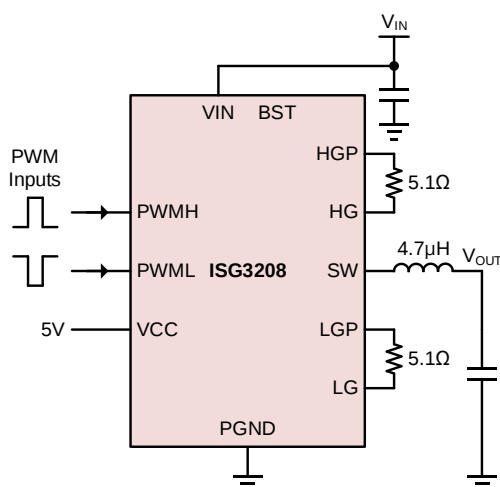


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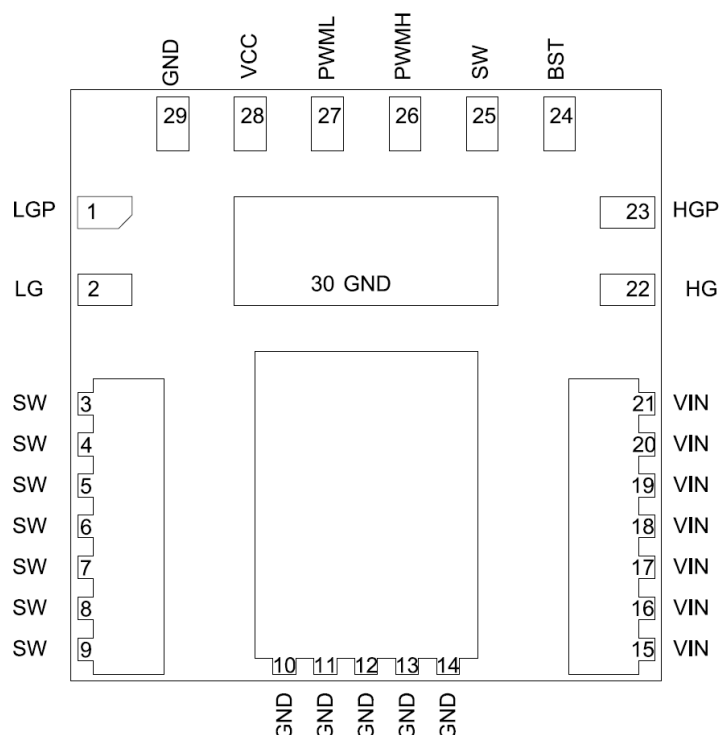
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5. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2025-09-09	Final datasheet release

6. Pin Configuration and Functions



30-Lead En-LGA (6.5mm x 6.5mm) Package – Top View

Pin Number	Pin Name	Description
1	LGP	Low-Side Gate Driver Source-Current Output. An optional resistor between LGP and LG can be employed to adjust turn-on speed of low side GaN FET.
2	LG	Low-Side Gate Terminal.
3-9	SW	Switching Node for Main Power.
10-14, 29-30	GND	Power Ground.
15-21	VIN	Input Voltage Supply. Locally bypass this pin to GND with ceramic capacitors
22	HG	High-Side Gate Terminal.
23	HGP	High-Side Gate Driver Source-Current Output. An optional resistor between HGP and HG can be employed to adjust turn-on speed of high side GaN FET.
24	BST	High-Side Gate Driver Bootstrap Rail. A 0.1uF ceramic capacitor is integrated between BST and SW pins, and external bootstrap capacitor is optional.
25	SW	Switching Node for Gate Drive Loop. SW waveform can be monitored. Pin 25 is connected to Pin 3-9 internally and no external connection is necessary.
26	PWMH	High-Side Driver PWM Input. This pin has an internal 200kΩ pull-down resistor.
27	PWML	Low-Side Driver PWM Input. This pin has an internal 200kΩ pull-down resistor.
28	VCC	External 5V Driver Supply. A 0.1uF ceramic capacitor is integrated between VCC and GND pins, and external decoupling capacitor is optional.

7. Absolute Maximum Ratings

All pins are referred to GND pins, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device reliability and lifetime.

Parameter	Min	Max	Unit
Drain-to-Source Voltage of Internal GaN FET		100	V
VIN		100	V
VCC, BST to SW	-0.3	6.0	V
SW	-5	100	V
BST	-0.3	105	V
HGP, HG	$V_{SW}-0.3$	$V_{BST}+0.3$	V
LGP, LG	-0.3	6.0	V
PWMH, PWML	-0.3	6.0	V
Continuous Current for Internal GaN FET		45 ⁽¹⁾	A
Pulsed Current for Internal GaN FET (25°C, $T_{Pulse} = 100 \mu s$)		230	A
Operating Junction Temperature T_J	-40	150	°C
Storage Temperature	-40	150	°C

(1) Ideal thermal condition. In real application the current capability depends on system thermal design.

8. ESD Ratings

Parameter	Value	Unit
Human Body Model (HBM), per JESD22-A114 ⁽²⁾	±1500	V
Charged Device Model (CDM), per JESD22-C101F ⁽³⁾	±1000	V

(2) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP155 states that 250V CDM allows safe manufacturing with a standard ESD control process.

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
VIN	0	80	V
VCC	4.5	5.5	V
PWMH, PWML	0	5.5	V
SW	-4	80	V
BST	$SW+4.5$	$SW+5.5$	V
SW Slew Rate		50	V/ns
Operating Junction Temperature T_J	-40	125	°C

10. Thermal Information

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	30.19	°C/W
$R_{\theta JC(TOP)}$	Thermal Resistance, Junction to Case Top	0.24	°C/W
$R_{\theta JC(BOT)}$	Thermal Resistance, Junction to Case Bottom	4.27	°C/W
T_{sold}	Maximum Reflow Soldering Temperature	≤260	°C

* $R_{\theta JA}$ is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is

mounted in horizontal position without air stream cooling.

11. Electrical Characteristics

$T_J = 25^\circ\text{C}$, $V_{CC} = BST = 5\text{V}$, $SW = GND = 0\text{V}$, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Input						
VCC Quiescent Current	I_{CC-Q}		35	60	μA	PWMH = PWML = 0
VCC Operating Current	I_{CC-OP}		10	20	mA	$f = 1\text{MHz}$
BST Quiescent Current	I_{BST-Q}		40	70	μA	PWMH = PWML = 0
BST Operating Current	I_{BST-OP}		10	20	mA	$f = 1\text{MHz}$
VCC Overvoltage Rising Threshold	V_{CC-OVR}	5.7	6	6.3	V	
VCC Overvoltage Hysteresis	$V_{CC-OVHYS}$		0.25		V	
VCC Undervoltage Rising Threshold	V_{CC-UVR}	3.9	4.1	4.3	V	
VCC Undervoltage Hysteresis	$V_{CC-UVHYS}$		0.3		V	
BST Undervoltage Rising Threshold	$V_{BST-UVR}$		3.6		V	
BST Undervoltage Hysteresis	$V_{BST-UVHYS}$		0.5		V	
PWM Input						
Input High Threshold	V_{IH}		1.8	2.2	V	
Input Low Threshold	V_{IL}	0.8	1.2		V	
Input Hysteresis	V_{I-HYS}		0.6		V	
Input Pull-Down Resistance	R_I		200		k Ω	
Bootstrap Switch						
Switch On Resistance	$R_{BST(ON)}$		4		Ω	
High and Low-Side Gate Driver						
Output Pull-Down Resistance	R_{DN}		0.2	1	Ω	I_{HG} or $I_{LG} = 10\text{mA}$
Output Pull-Up Resistance	R_{UP}		1	2	Ω	I_{HGP} or $I_{LGP} = -10\text{mA}$
Output Peak Source Current ⁽⁴⁾	I_{OH}		1.7		A	HGP = SW or LGP = GND
Output Peak Sink Current ⁽⁴⁾	I_{OL}		4.3		A	HG = BST or LG = VCC
Over Temperature Protection						
OTP Shutdown Rising Threshold ⁽⁴⁾	T_{OTP}		165		$^\circ\text{C}$	
OTP Shutdown Hysteresis ⁽⁴⁾	$T_{OTP-HYS}$		20		$^\circ\text{C}$	
GaN FETs						
Drain-to-Source Voltage	BV_{DSS}	100			V	PWML = 0V or PWMH = 0V, $I_D = 1500\mu\text{A}$
Drain-Source Leakage	I_{DSS}		1	100	μA	PWML = 0V or PWMH = 0V, $V_{DS} = 100\text{V}$
High-side GaN FET Drain-Source On Resistance	$R_{DS(ON)_HS}$		3.1	4	m Ω	PWMH = 5V, $I_D = 25\text{A}$
Low-side GaN FET Drain-	$R_{DS(ON)_LS}$		2.7	3.6	m Ω	PWML = 5V, $I_D = 25\text{A}$

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Source On Resistance						
Source-Drain Forward Voltage	V_{SD}		1.3		V	PWML = 0V or PWMH = 0V, $I_S = 0.5A$
Input Capacitance ⁽⁴⁾	C_{ISS}		950		pF	PWML = 0V or PWMH = 0V, $V_{DS} = 50V$
Output Capacitance ⁽⁴⁾	C_{OSS}		405			
Reverse Transfer Capacitance ⁽⁴⁾	C_{RSS}		8			
Energy Related C_{OSS} ⁽⁴⁾	$C_{OSS(ER)}$		575		pF	PWML = 0V or PWMH = 0V, $V_{DS} = 0V$ to 50V
Time Related C_{OSS} ⁽⁴⁾	$C_{OSS(TR)}$		805			
Total Gate Charge ⁽⁴⁾	Q_G		8		nC	PWML = 0V or PWMH = 0V, $V_{DS} = 0V$ to 50V, $I_D = 25A$
Output Charge ⁽⁴⁾	Q_{OSS}		40			PWML = 0V or PWMH = 0V, $V_{DS} = 0V$ to 50V

12. Switching Characteristics

$T_J = 25^\circ C$, $V_{CC} = BST = 5V$, $SW = GND = 0V$, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Minimum Input Pulse Width that Changes the Output ⁽⁴⁾	T_{IPW}		10		ns	
Minimum Gate Output Pulse Width ⁽⁴⁾	T_{OPW}		12		ns	
HGP Rise Time (0.5V-4.5V) ⁽⁴⁾	T_{R_SW}		10		ns	
HG Fall Time (4.5V-0.5V) ⁽⁴⁾	T_{F_SW}		3		ns	
LGP Rise Time (0.5V-4.5V) ⁽⁴⁾	T_{R_LS}		10		ns	
LG Fall Time (4.5V-0.5V) ⁽⁴⁾	T_{F_LS}		3		ns	
Dead time – LG off to HGP on ⁽⁴⁾	T_{DTH}		1		ns	
Dead time – HG off to LGP on ⁽⁴⁾	T_{DTL}		1		ns	
HG Turn-Off Propagation Delay ⁽⁴⁾	T_{HPLH}		20		ns	PWMH falling to HG falling
HGP Turn-On Propagation Delay ⁽⁴⁾	T_{HPLH}		20		ns	PWMH rising to HGP rising
LG Turn-Off Propagation Delay ⁽⁴⁾	T_{LPHL}		20		ns	PWML falling to LG falling
LGP Turn-On Propagation Delay ⁽⁴⁾	T_{LPLH}		20		ns	PWML rising to LGP rising
Delay Matching LGP On and HG Off ⁽⁴⁾	T_{MON}		1		ns	
Delay Matching LG Off and HGP On ⁽⁴⁾	T_{MOFF}		1		ns	

(4) Not 100% tested and guaranteed by design.

13. Typical Characteristics

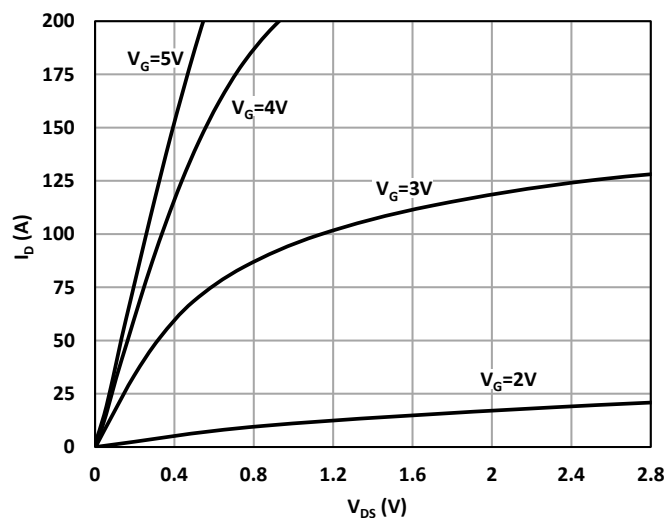


Figure 1. Pulsed Drain Current vs. Drain Voltage (25°C)

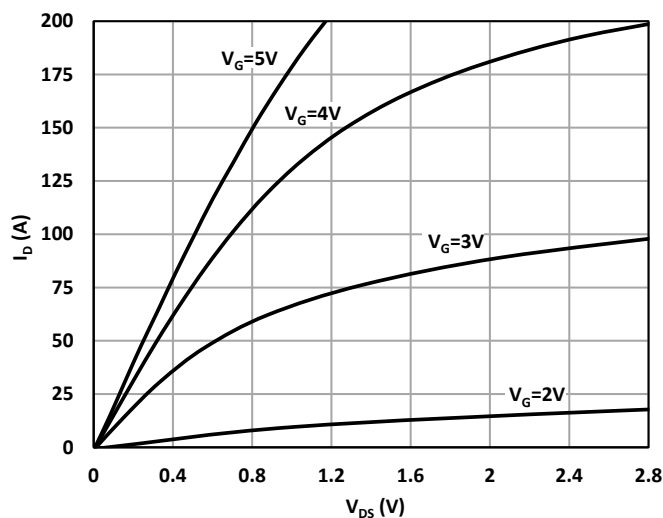


Figure 2. Pulsed Drain Current vs. Drain Voltage (125°C)

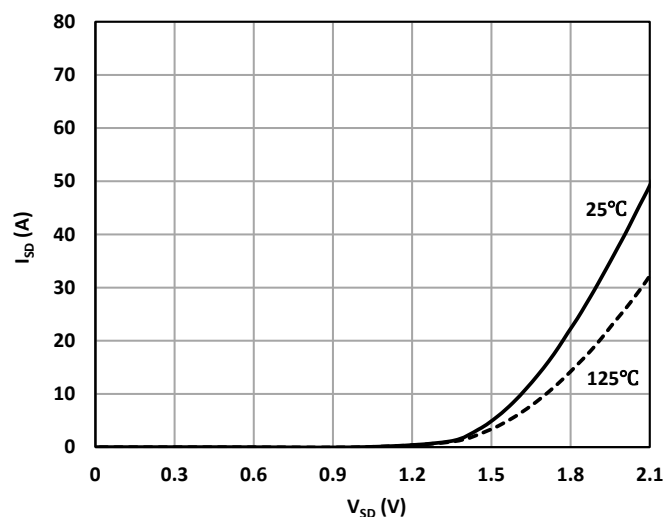


Figure 3. Source-Drain Reverse Conduction Voltage

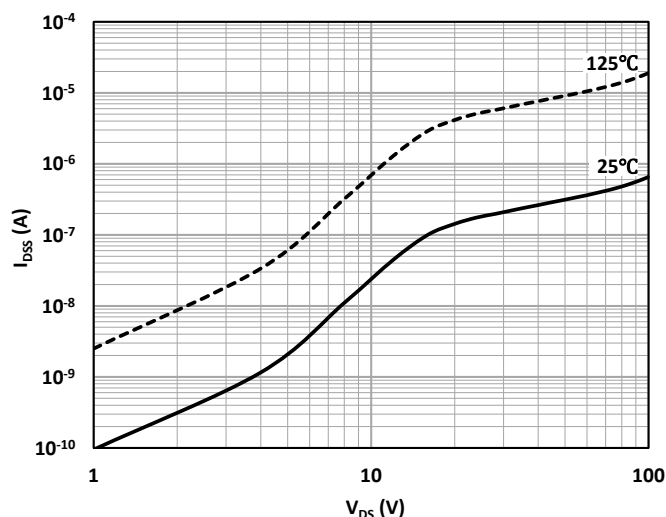


Figure 4. Drain Leakage Current vs. Drain Voltage

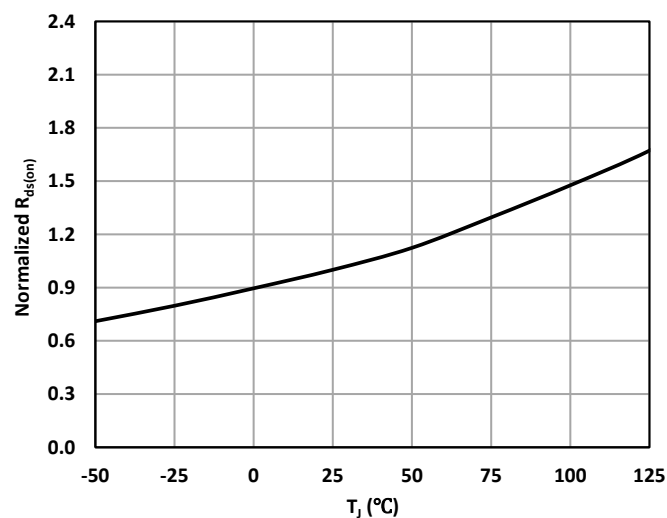


Figure 5. Normalized $R_{DS(ON)}$ vs Temperature

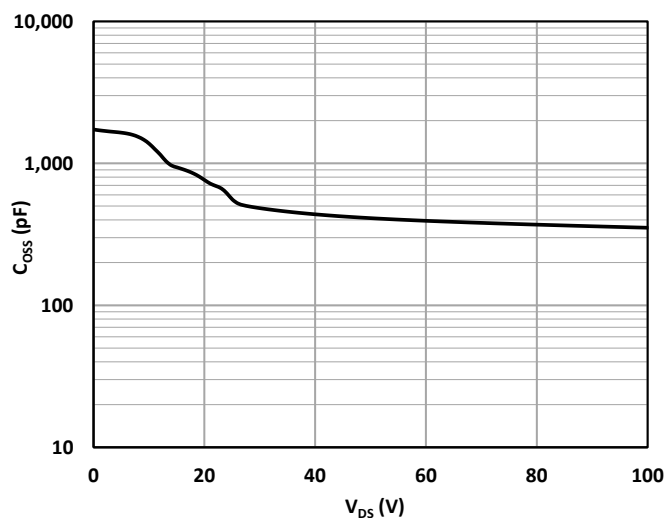


Figure 6. Output Capacitance vs Drain Voltage

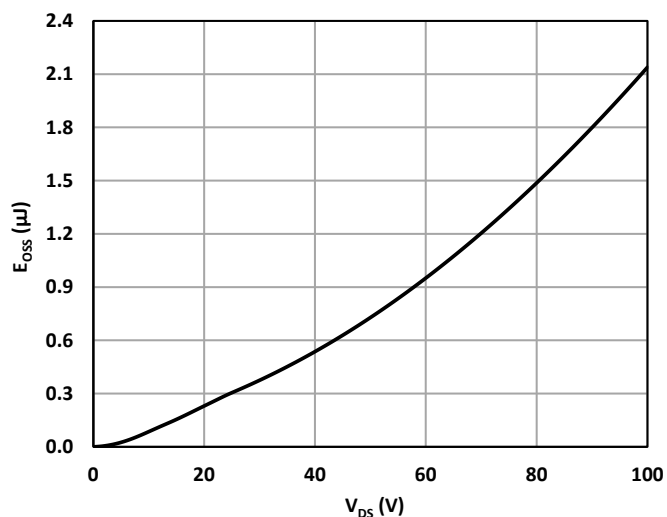


Figure 7. Output Capacitance Stored Energy vs Drain Voltage

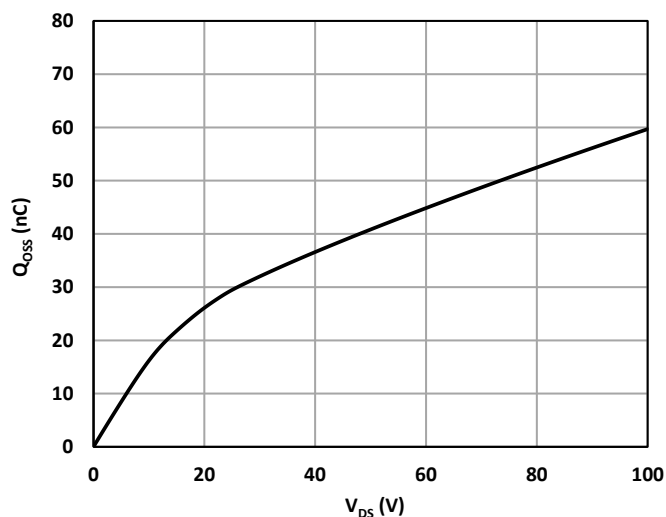


Figure 8. Output Charge vs Drain Voltage

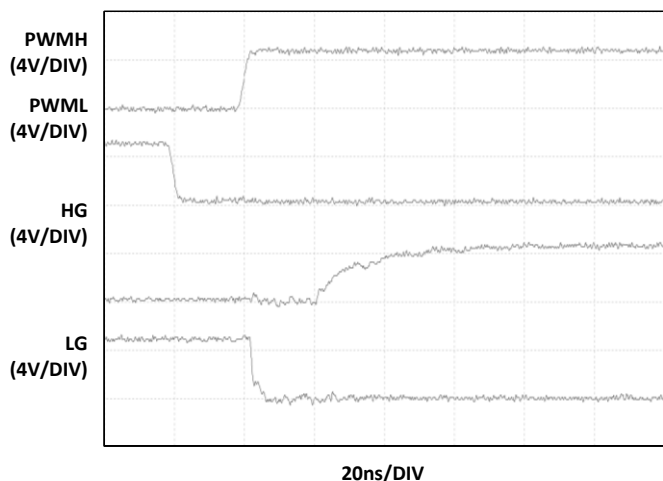


Figure 9. HG Turn-On and LG Turn-Off Waveform with 5.1Ω external gate resistors

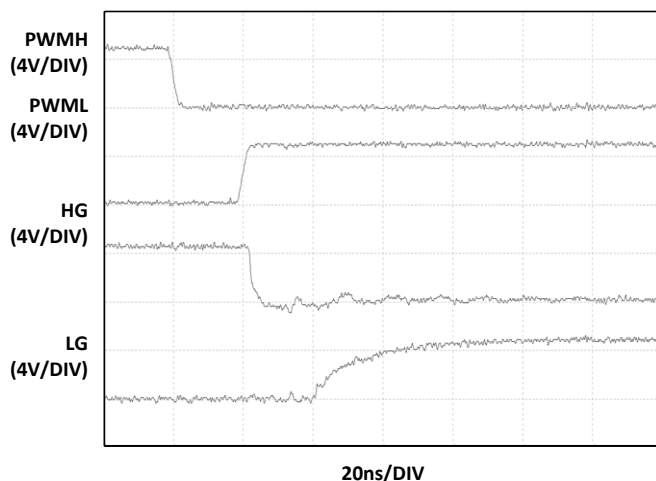


Figure 10. HG Turn-Off and LG Turn-On Waveform with 5.1Ω external gate resistors

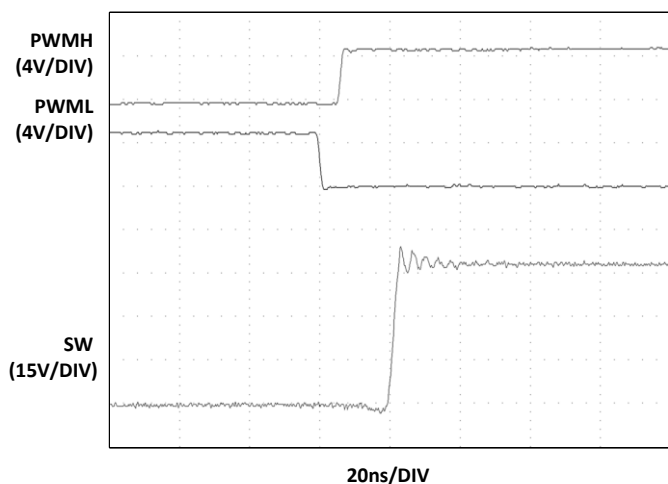


Figure 11. SW Rising Waveform at $V_{IN}=48V$ and $I_{OUT}=20A$

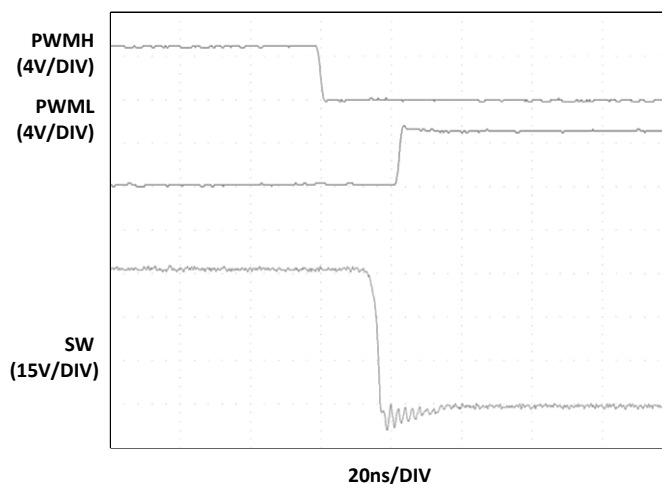


Figure 12. SW Falling Waveform at $V_{IN}=48V$ and $I_{OUT}=20A$

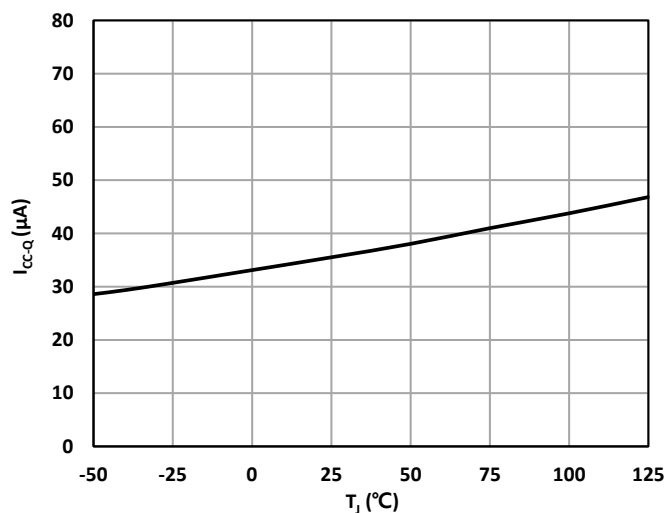


Figure 13. VCC Quiescent Current vs Temperature

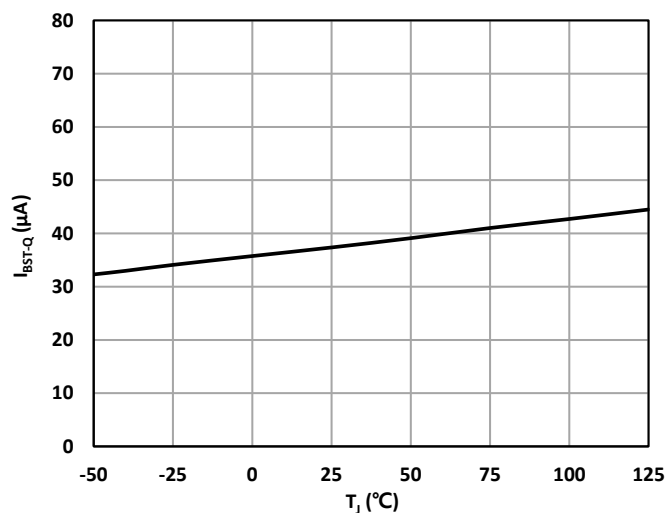


Figure 14. BST Quiescent Current vs Temperature

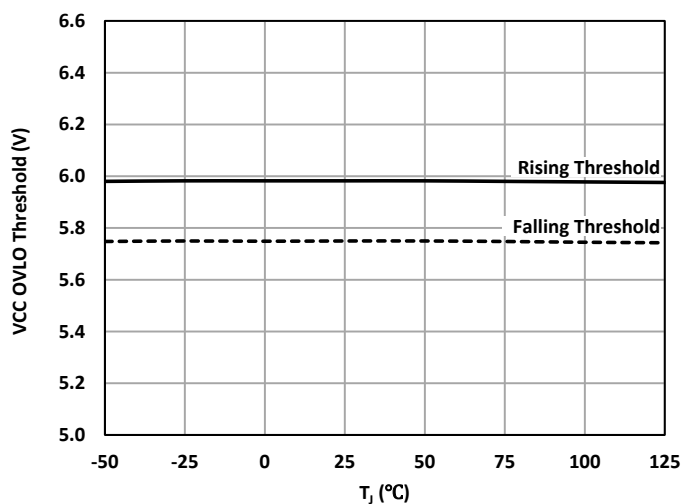


Figure 15. VCC OVLO Threshold vs Temperature

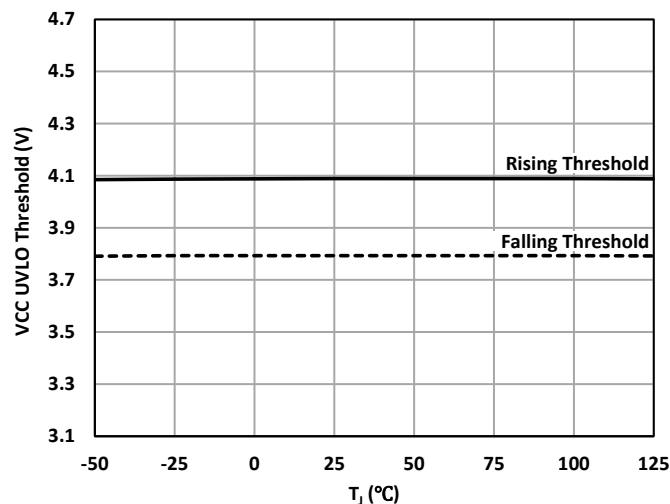


Figure 16. VCC UVLO Threshold vs Temperature

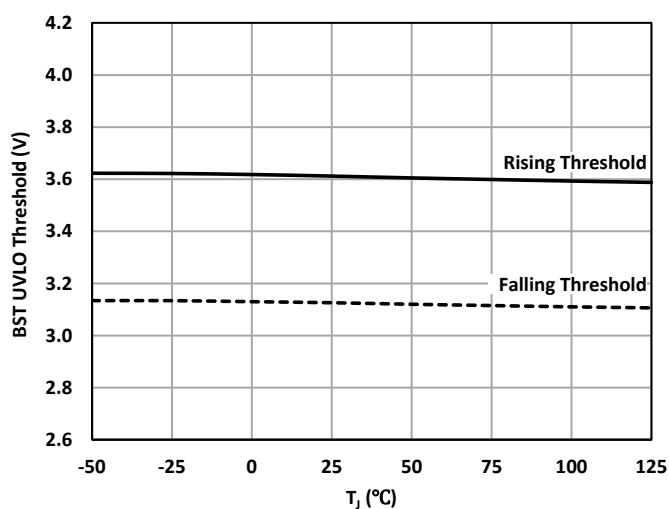


Figure 17. BST UVLO Threshold vs Temperature

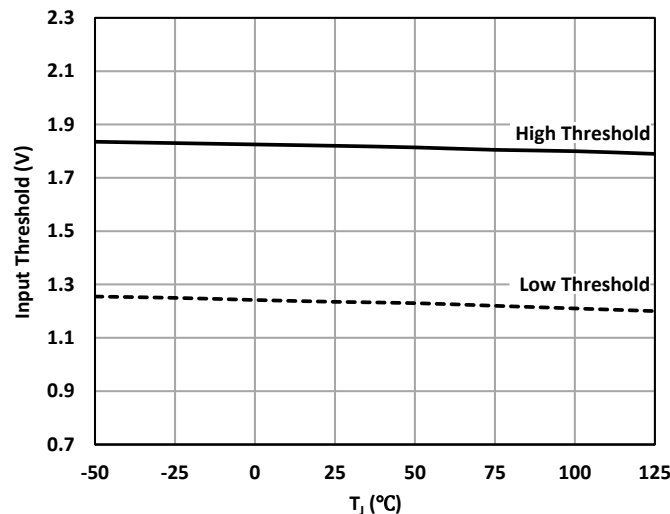


Figure 18. PWM Input Threshold vs Temperature

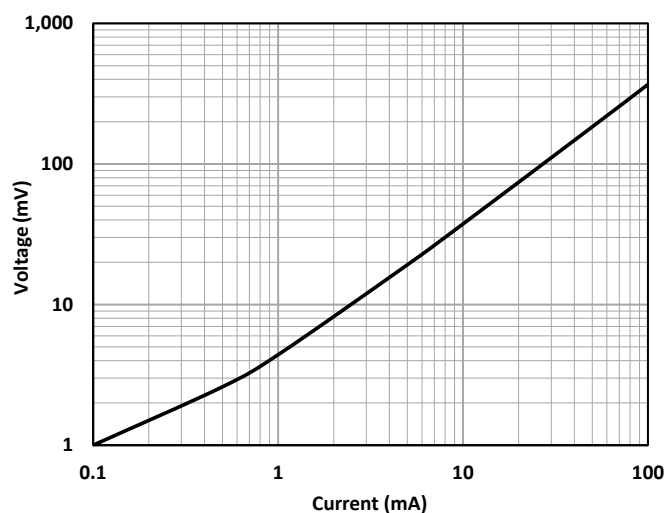


Figure 19. Bootstrap Forward Voltage vs Current

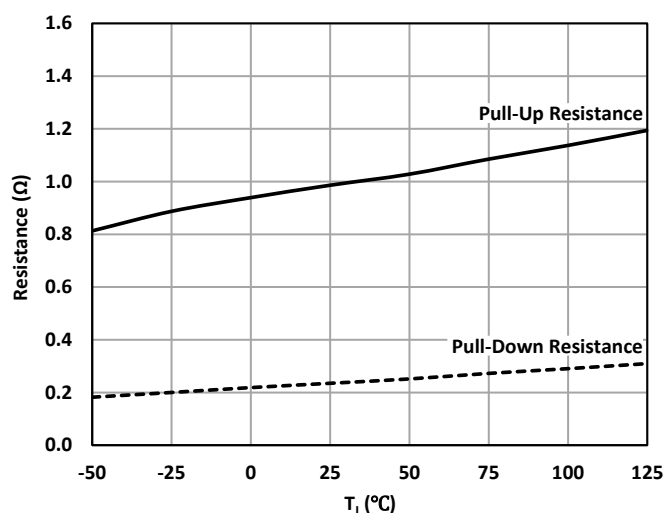


Figure 20. Output Pull-Down/Pull-Up Resistance vs Temperature

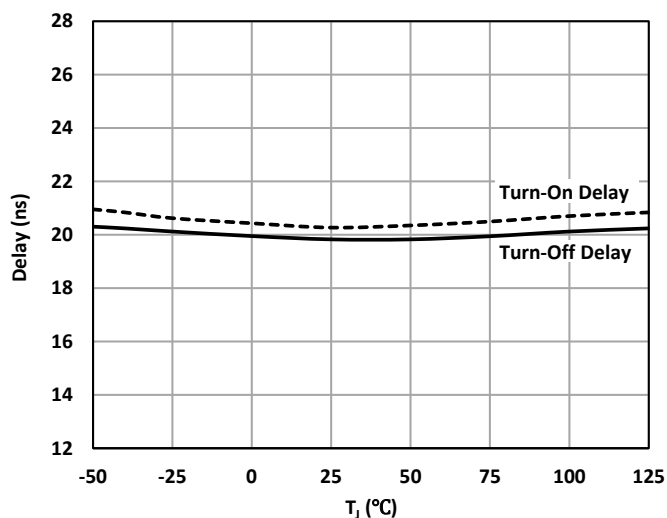


Figure 21. Low-Side Propagation Delay vs Temperature

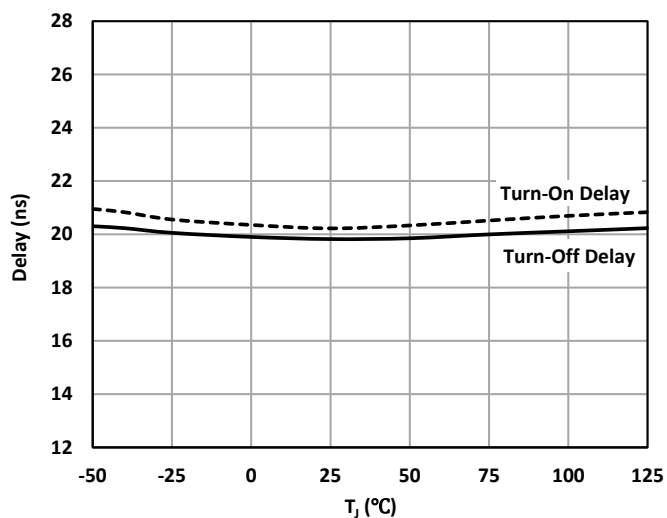


Figure 22. High-Side Propagation Delay vs Temperature

14. Block Diagram

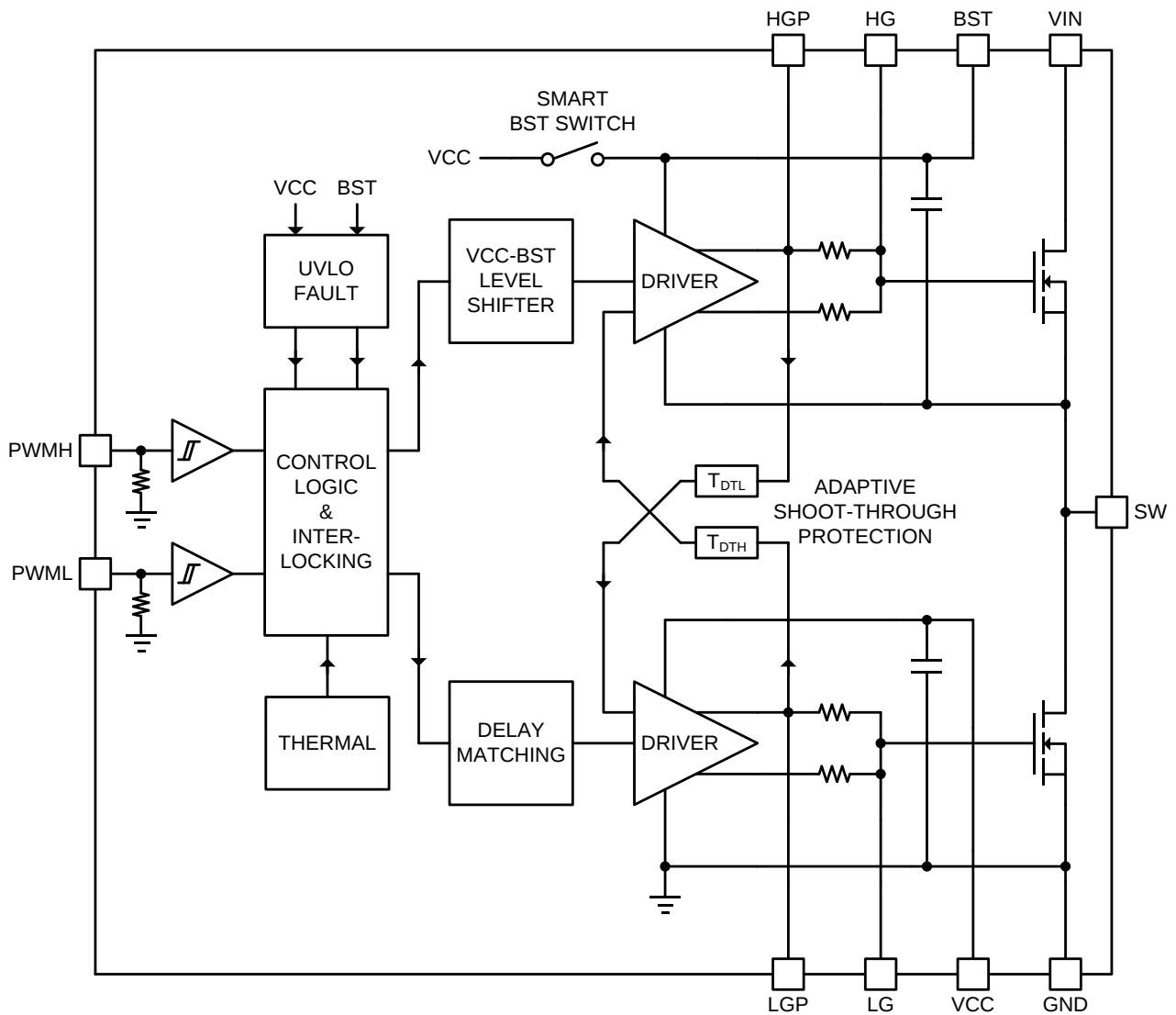


Figure 23. Functional Block Diagram

15. Function Description

The ISG3208 is a 100V SolidGaN half-bridge module in a compact 6.5mm x 6.5mm LGA package. Within that tiny package, it integrates two high-performance enhancement-mode GaN FETs, gate drivers, gate resistors, and VCC and BST supply capacitors, offering the smallest, most efficient, and easy-to-use GaN power stage solution.

The ISG3208 features two independent and TTL logic compatible inputs to offer control flexibility. It provides split gate driver outputs for the independent control of turn-on and turn-off speeds of both high-side and low-side GaN FETs by adding external gate resistors. The ISG3208's PWM input interlocking function with integrated adaptive shoot-through protection ensures neither output conducts simultaneously, even under near zero dead time delay conditions. Active bootstrap (BST) voltage control in ISG3208 prevents overcharging of the BST supply during dead times, protecting the gate of the GaN FET. Additionally, rich fault protection is provided including independent VCC and BST undervoltage lockout (UVLO), VCC overvoltage lockout (OVLO), and over temperature protection (OTP). Highly integrated with ultra-low inductance, fast propagation delay, and superior dV/dt immunity, the ISG3208 drives next-generation high-frequency, high-power-density applications across diverse topologies including buck, boost, and buck-boost.

Input and Output

The ISG3208 input pins, PWMH and PWML, are independent and TTL logic compatible with the ability to withstand input voltages up to 5.5V regardless of VCC voltage. The ISG3208 offers fast propagation delay (20ns typical) with excellent delay matching (1ns typical) between the high-side and low-side driver channels, making it ideal for high-frequency applications. Both inputs feature a 10ns (typical) input deglitch filter to remove any unwanted pulses from a PWM input. A narrow input pulse exceeding this deglitch delay time will be extended to a minimum output pulse of 12ns (typical) to ensure proper gate turn-on and turn-off transients. Figure 24 shows the switching characteristics of the input and output. The ISG3208 features the interlocking function to prevent shoot-through condition. When both input pins, PWMH and PWML, are high, the internal logic turns off both output pins, HG and LG, as illustrated in Figure 25. Both input pins have an internal pull-down resistor of 200k Ω . Table 1 shows the truth table of input and output.

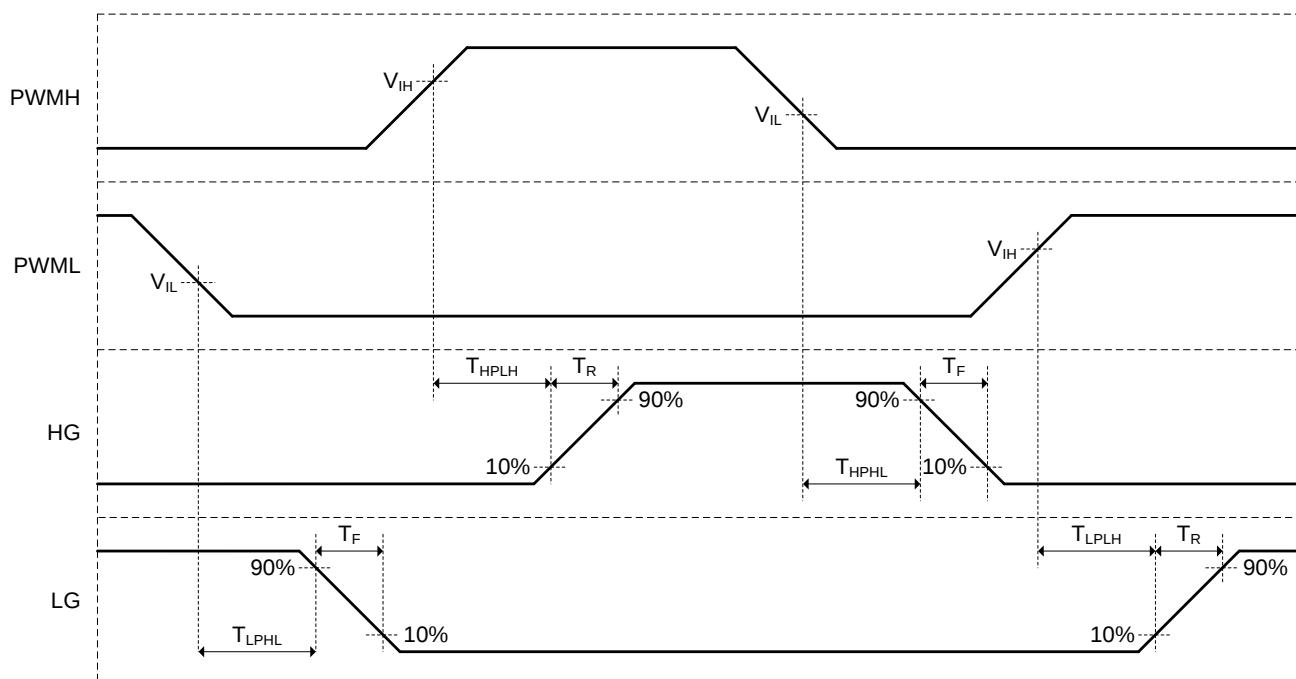


Figure 24. Timing Diagram of Input and Output

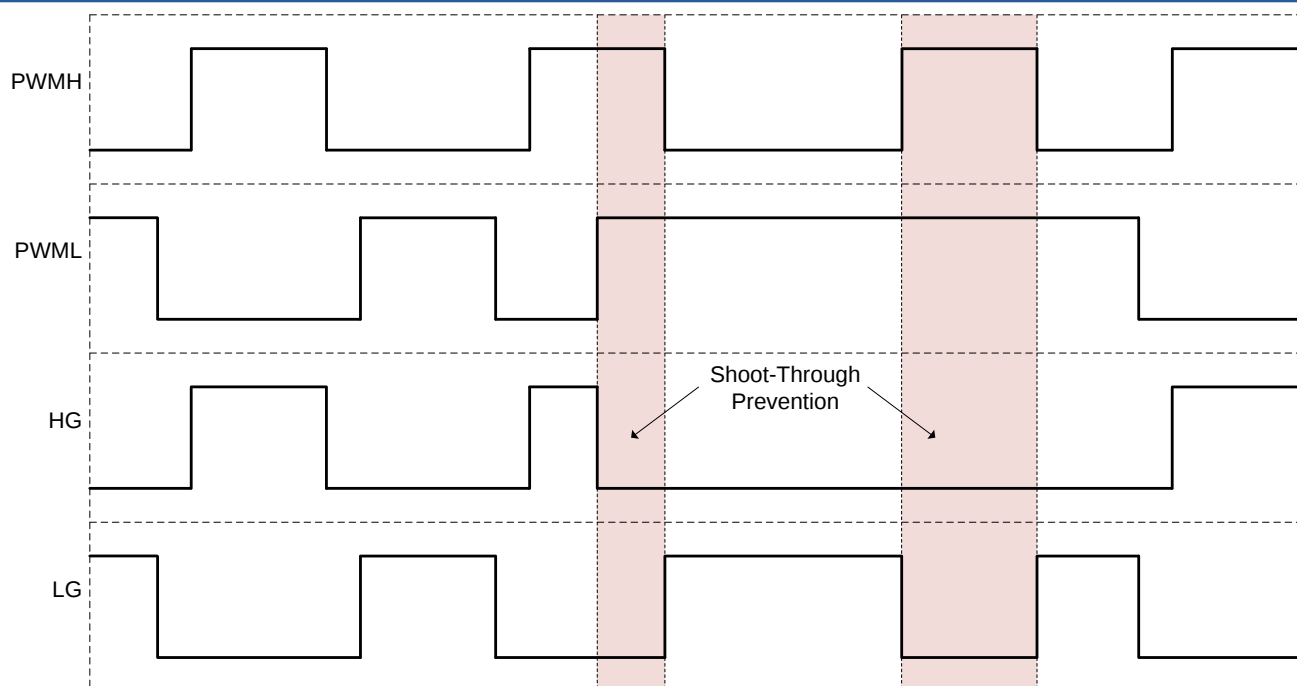


Figure 25. Timing Diagram of Interlocking Function

Table 1. Input and Output Truth Table

PWMH	PWML	HG	LG	Comment
H	L	H	L	High-Side GaN FET On
L	H	L	H	Low-Side GaN FET On
L	L	L	L	Both GaN FETs Off
H	H	L	L	Both GaN FETs Off

Adaptive Shoot-Through Protection

The ISG3208 features an internal shoot-through protection circuit, leveraging shunt sensing of the true gate voltage of GaN FETs through its split outputs structure. It offers precise switching timing control for immediate turn-on after complete turn-off of the opposite side to ensure that they do not conduct simultaneously in any situation. This is processed within a 1ns (typical) to achieve that near-zero dead time delay enhancing efficiency and enabling high-frequency operation.

Half-Bridge Output Stage

The ISG3208 integrates 3.1mΩ(HS)/2.7mΩ(LS), 100V, enhancement-mode GaN FETs with drivers in a half-bridge configuration. It offers increased flexibility by providing split gate driver outputs for both high-side and low-side GaN FETs. As depicted in Figure 26, the internal gate drive output provides a default 20Ω internal pull-up resistor and a 1Ω internal pull-down resistor. Designers can further fine-tune turn-on strength by adding an external resistor in parallel between designated pins of HGP/HG and/or LGP/LG. While turning-off the GaN FET, the integrated strong 0.2Ω pull-down FET offers a robust, low impedance path necessary for eliminating high dv/dt induced gate turn-on. Additionally, the ISG3208 integrates the 0.1μF BST and VCC supplies capacitors within the package, thereby significantly reducing parasitic inductance loop paths and effectively minimizing voltage spikes at the gates of the GaN FETs. HG and LG pins have internal 50kΩ pull-down resistors to SW and GND, respectively.

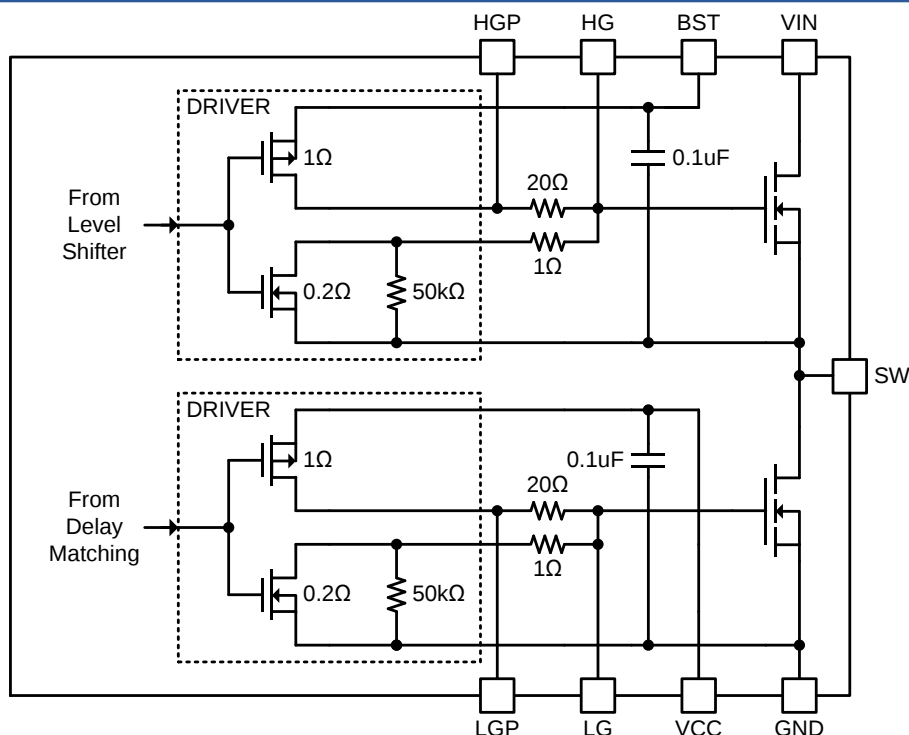


Figure 26. Simplified Output-Stage Block Diagram

VCC UVLO/OVLO Protections

The ISG3208 features UVLO and OVLO for VCC, providing the operation under the safe conditions of devices. When the VCC voltage falls below its UVLO threshold of 3.8V (typical) or exceeds above its OVLO threshold of 6.0V (typical), the ISG3208 turns off both the high-side and low-side GaN FETs and ignores the PWMH and PWML inputs.

High dv/dt Rate GaN FET Switching

GaN FETs can switch much faster than traditional silicon based MOSFETs, requiring gate drivers capable of delivering precise and fast switching signals to fully leverage their potential. Managing high dv/dt rates during switching is important for stable gate driver circuitry, ensuring reliable and efficient operation. The ISG3208 features an advanced level-shifting technology circuit designed to overcome these challenges associated with driving GaN FETs. Its advanced noise rejection mechanism ensures precise and accurate signal transmission between the control logic to driver outputs even in extreme high dv/dt environments up to 50V/ns.

Another challenge in driving GaN FETs is the issue of high reverse conduction voltage. When the SW node drops below 0V due to this reverse conduction, it can temporarily lower the level shifter's supply rail, causing a disruption in the level shifter's output signals. This disruption can appear as a delay mismatch between signals transmitted to each side of the driver, resulting in timing inaccuracies and potential performance degradation. The proposed level shifter in the ISG3208 is designed to prevent such conditions, ensuring that delay variation is kept to a minimum (1ns typical) even when the SW node fluctuates by up to -4V. Furthermore, the ISG3208 features an additional delay matching circuit that parallels the proposed level shifter circuit, matching its process and temperature variation characteristic. This additional feature further improves delay matching to 1ns (typical).

High-Side Gate-Driver Supply

Despite GaN devices offering advantages with their superior figure of merit ($Q_G \times R_{DS(on)}$) compared to silicon based MOSFET counterparts, their sensitivity to gate driving voltage levels presents a challenging concern. GaN devices are more vulnerable to both over-voltage and under-voltage conditions at the gate, which can have negative effects on their reliability and performance. The concern over gate over-voltage is more significant for GaN FETs, given that they are considerably more fragile compared to their silicon counterparts. Conversely, Insufficient gate voltage, or gate under-voltage, can result in increased switching losses and reduced efficiency.

To mitigate these challenges, the ISG3208 features a smart BST switch that allows precise control for BST charging and blocking. Figure 27 illustrates the operation principle of the smart BST switch. Unlike silicon MOSFETs, GaN FETs typically lack an intrinsic body diode, resulting in higher reverse conduction voltages, (typically 2V to 3V or even higher at high current) during dead time. This can lead to overcharging of the BST capacitor, potentially causing permanent damage to the gate of the high-side GaN FET. In the ISG3208, the BST switch's turning on and off are precisely controlled so that it allows charging of the BST capacitor only during SW node is fully reached at GND voltage when the low-side power switch is being turned on. Moreover, the BST switch exhibits a low on-impedance of 4Ω (typical), ensuring minimal dropout voltage. Accordingly, the ISG3208 always maintains a well-balanced BST rail voltage close to VCC, achieving excellent delay matching and balanced gate driving strength between the high-side and low-side drivers.

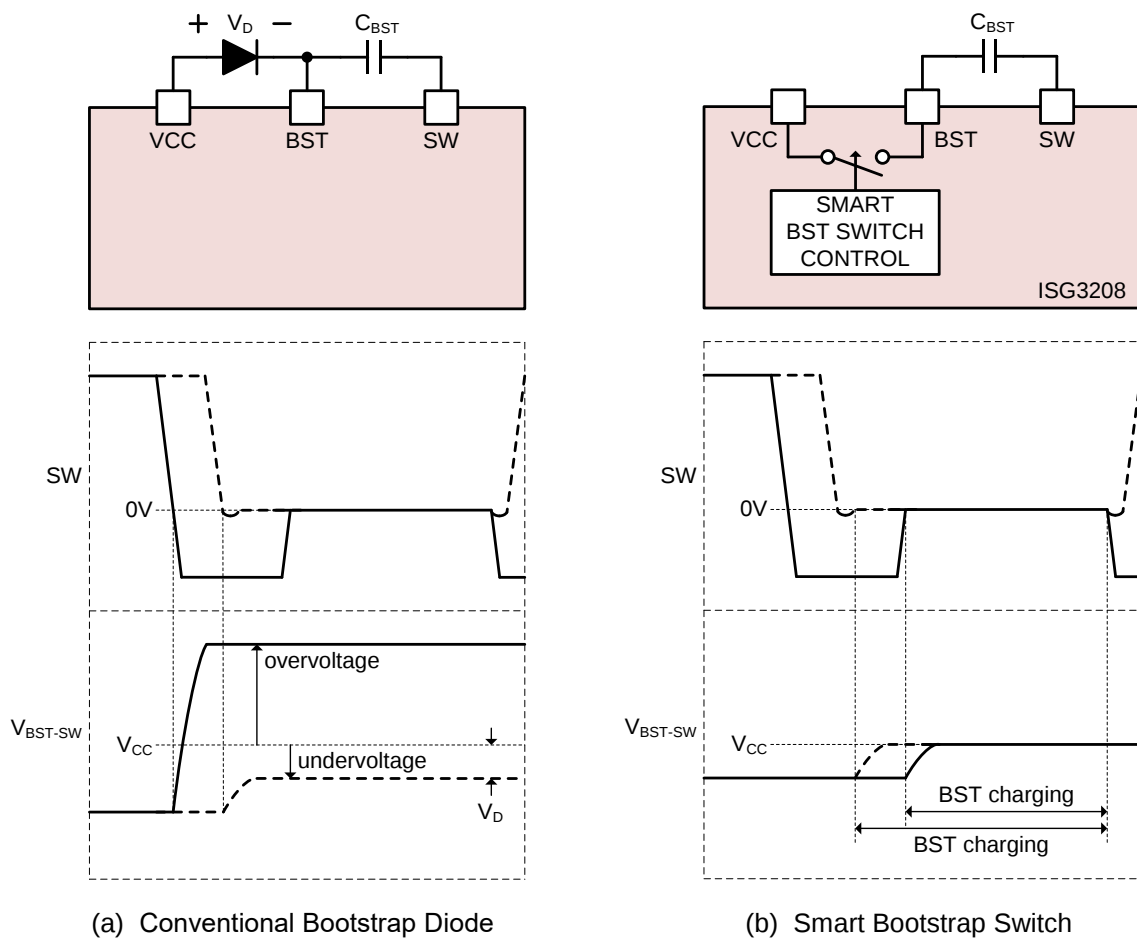


Figure 27. Operation Principle of Bootstrap Supply

Additionally, the ISG3208 provides a BST UVLO protection with a falling threshold of 3.1V (typical) and a rising threshold of 3.6V (typical). When BST-SW falls below BST UVLO threshold, the ISG3208 enters BST UVLO mode, turns off the high-side GaN FET, but the low-side driver and GaN FET remain activated.

Over Temperature Protection (OTP)

The ISG3208 employs OTP. If the internal junction temperature, T_j , exceeds 165°C (typical), The PWMH and PWML inputs are ignored, and both the high-side and low-side GaN FETs are turned off. When the temperature drops below 145°C (typical), the ISG3208 will resume normal operation.

Layout Recommendation

Due to the small input capacitance of the GaN FET, the ISG3208 can support a high-frequency operation but it causes high dv/dt and high di/dt in power loop. To avoid the voltage and current spike caused by high dv/dt and high di/dt, the parasitic of the gate driving loop and power loop must be reduced by proper layout technique.

The ISG3208 employs an excellent layout on internal substrate to reduce the gate driving loop and power loop: (1) The driver has been placed very close to the GaN FETs to minimize the loops of parasitic inductance and reduce the noise on the gate loop. (2) The bootstrap capacitor is integrated in the module and the distance between BST and VCC to the driver has been minimized to minimize power loop impedance. (3) The distance between high-side GaN FET and low-side GaN FET has been minimized to avoid excessive voltage spike to the driver caused by the parasitic inductance between high-side GaN FET and low-side GaN FET.

Although the optimized pinout of the ISG3208 simplifies the power stage layout significantly, a proper layout of PCB board is required to fully utilize the benefit of the ISG3208. The layout guidelines are as follows:

1. The optional resistor between HGP(LGP) pin and HG(LG) pin to adjust the turn-on speed of the GaN FETs should be placed close to ISG3208.
2. The optional VCC decoupling capacitor should be placed close to ISG3208.
3. Use planes for VIN and GND to minimize power losses and ensure effective voltage filtering. The power input decoupling capacitors should be placed close to ISG3208.

A 3-layer PCB layout example is shown in Figure 28. A two-layer board design is also possible due to the optimized pinout.

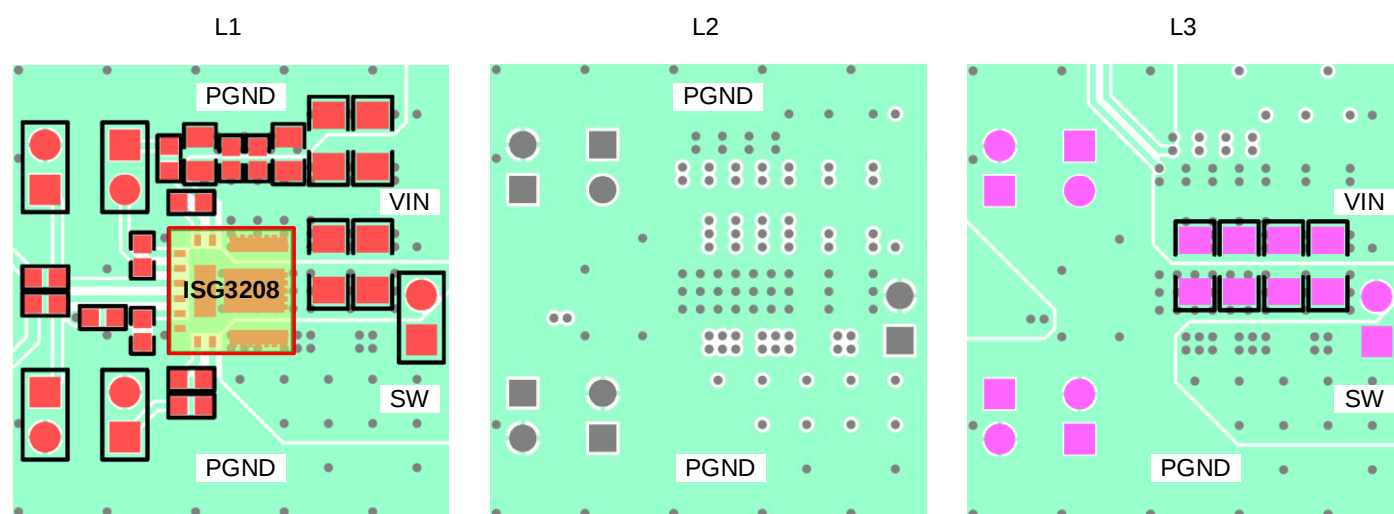


Figure 28. Three-Layer Layout Example

Typical Applications

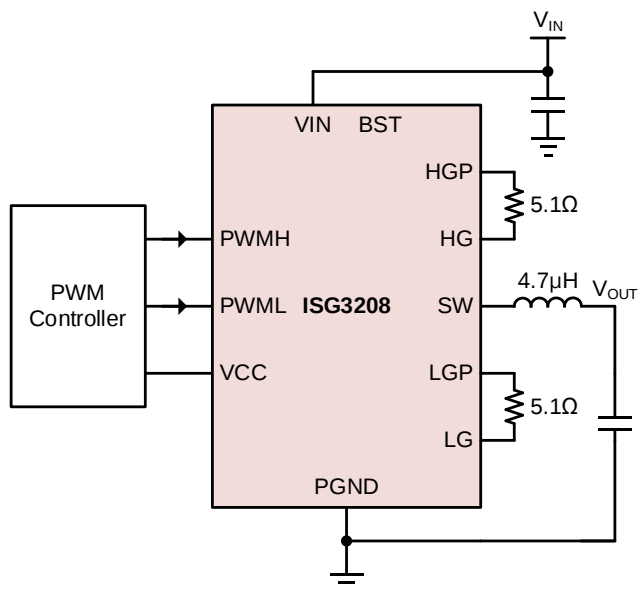


Figure 29. 36V – 80V Input, 12V Output, and 300W Buck Converter

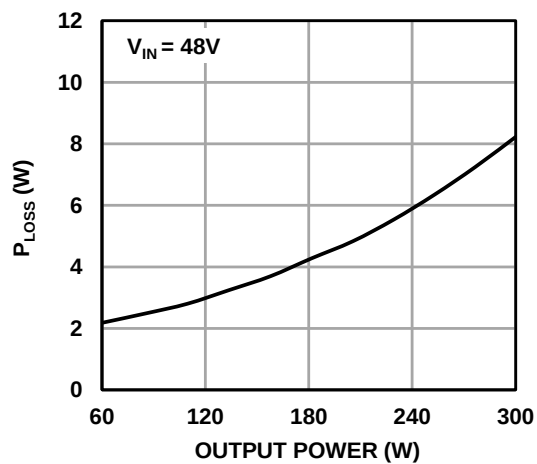
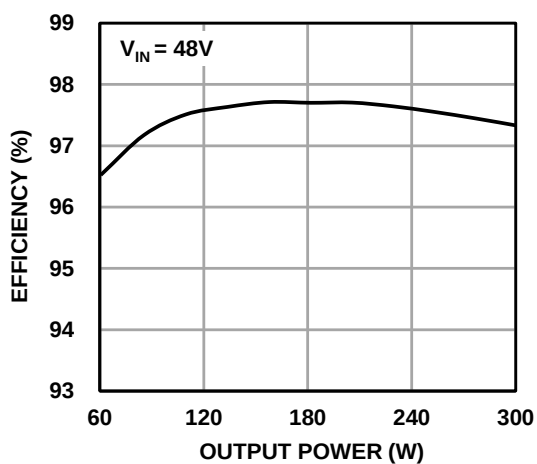
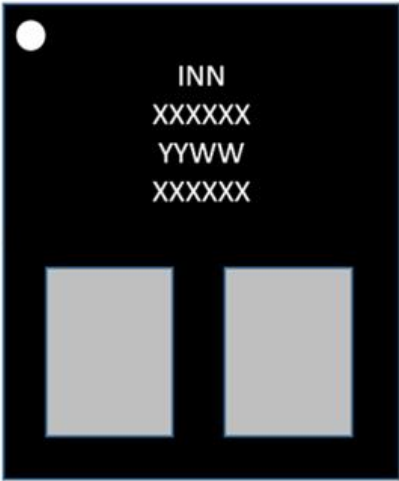
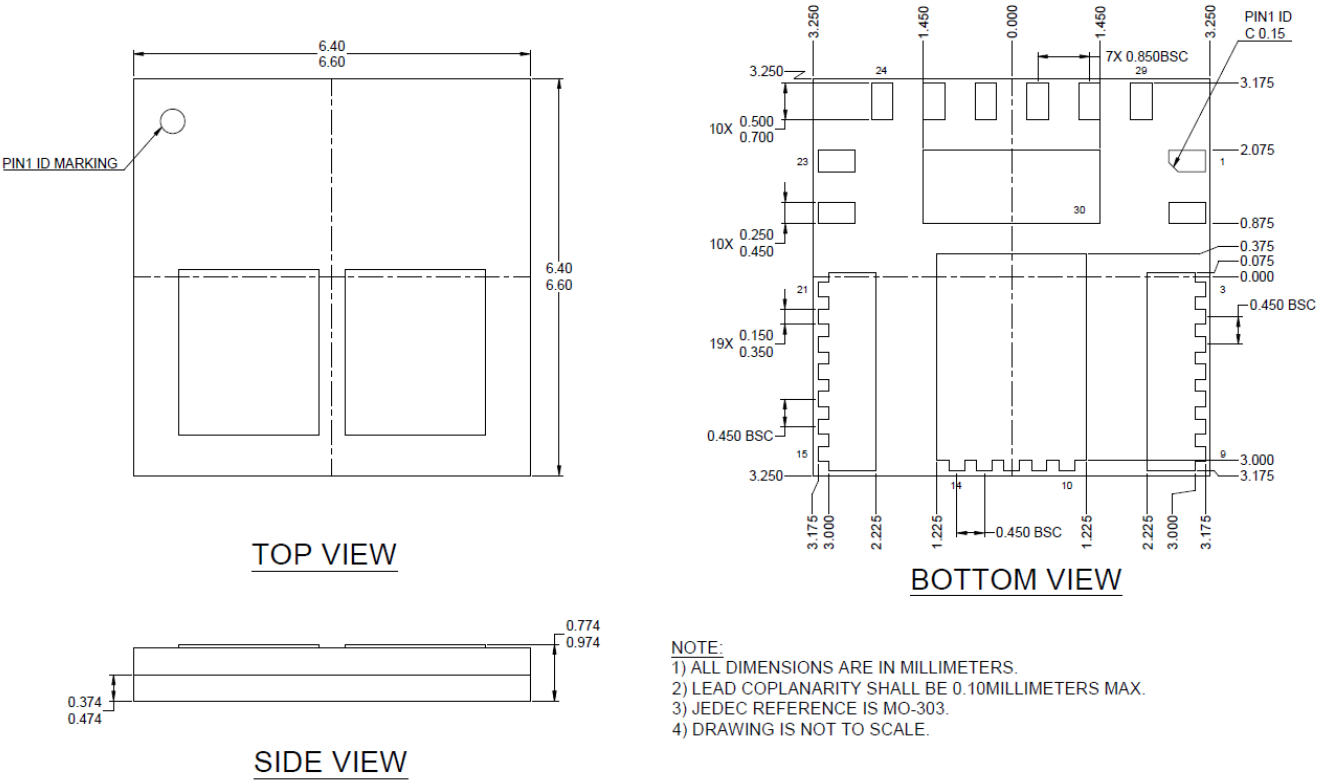


Figure 29. Efficiency vs Output Power and Power loss vs Output Power at $V_{OUT}=12V$: Refer to INNEHB100I1 Demo Board

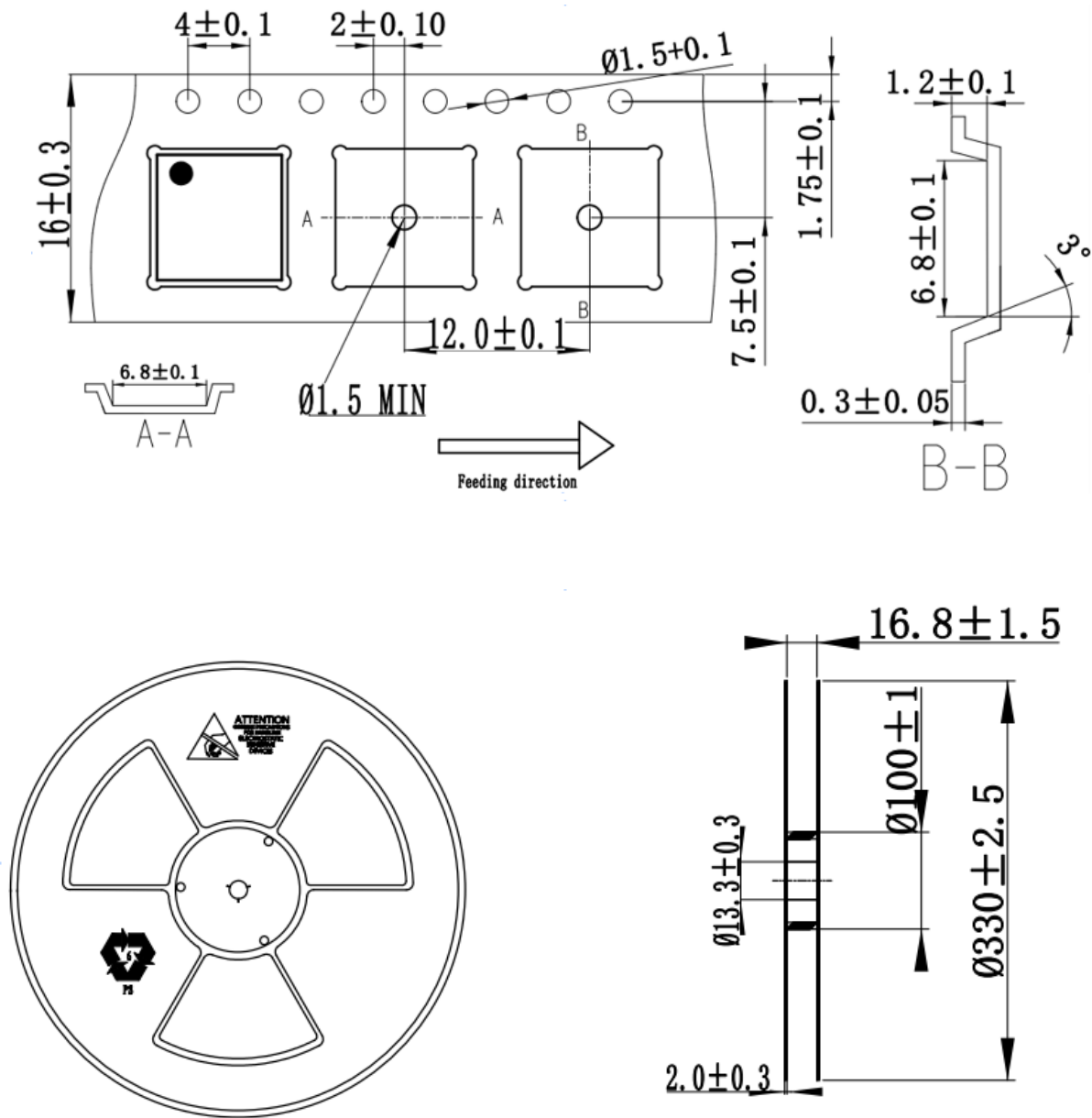
16. Package Information

En-LGA6.5X6.5 Package:



Row	Description	Example
Row1	Company Name	INN
Row2	Product Code	XXXXXX
Row3	Date Code	YYWW
Row4	Lot code	XXXXXX

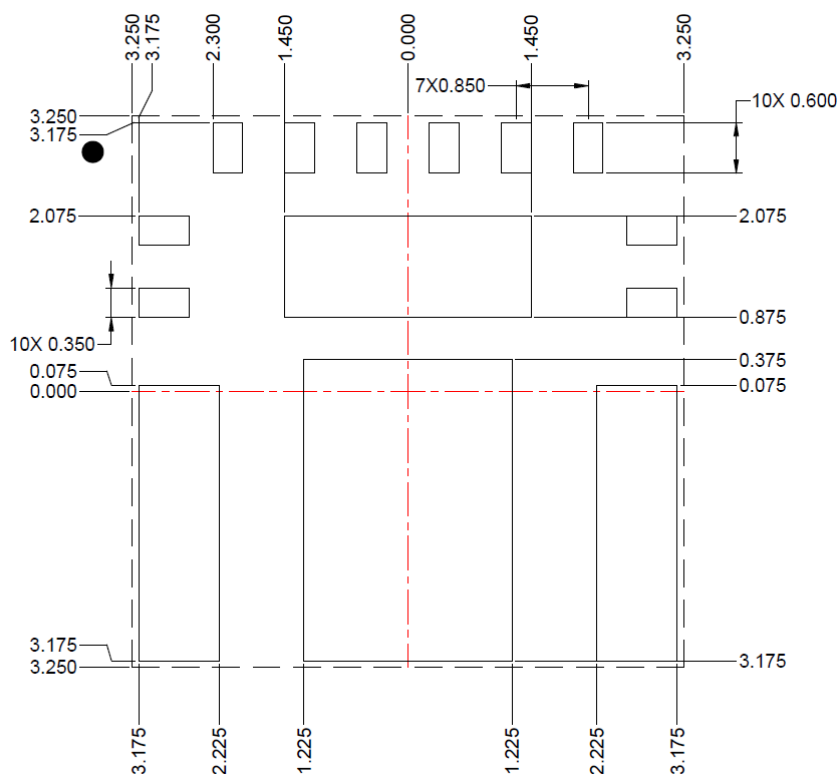
17. Tape and Reel Information



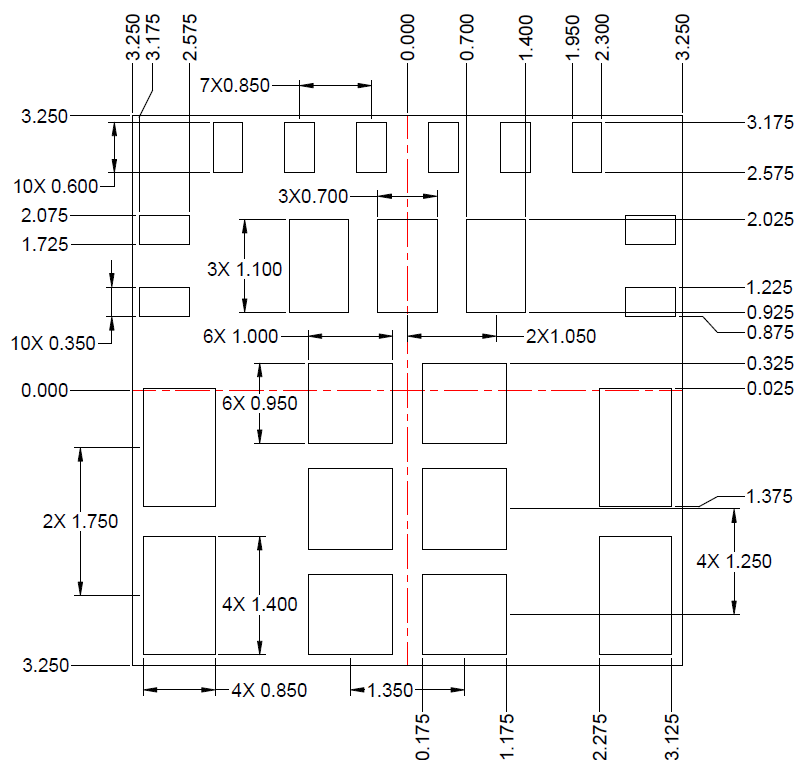
Note: All dimensions in mm.

18. Recommended Land Pattern

Recommended Land Pattern:



Recommended Stencil Drawing:



19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
ISG3208EA	En-LGA6.5x6.5-30L	3208EA	MSL3	13" 2500PCS/reel

Important Notice

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