

100V Low-Side Bi-Directional VGaN™ Driver

1. Features

- Compatible with AFE and MCU control logic
- 8uA Low Quiescent Current
- Special 5V GATE Drive Voltage for VGaN HEMT
- Fast Turn-On/-Off Speed
- Capable of Driving Multiple VGaN HEMTs in Parallel
- SOP 8-Lead Package

2. Applications

- Energy Storage System (ESS)
- E-Bike, E-Scooter
- Battery Backup and UPS
- Power and Gardening Tools
- Light Electric Vehicles (LEV)

3. Description

The INS1011 is designed to drive Innoscience's proprietary 40V to 120V VGaN, enhancement mode bi-directional GaN HEMT with single-gate dual-drain, for low-side battery protection in BMS systems. With strong drive capability, the INS1011 can drive multiple VGaN HEMTs in parallel within 100uSec. The CHG/DSG inputs are compatible with AFE and MCU control logic and can withstand input voltage up to 20V. The INS1011 is a special driver for 40V to 120V VGaN with 5V gate drive voltage. The INS1011 has fast turn-on and turn-off speed in response to fault condition to protect the system.

4. Typical Application

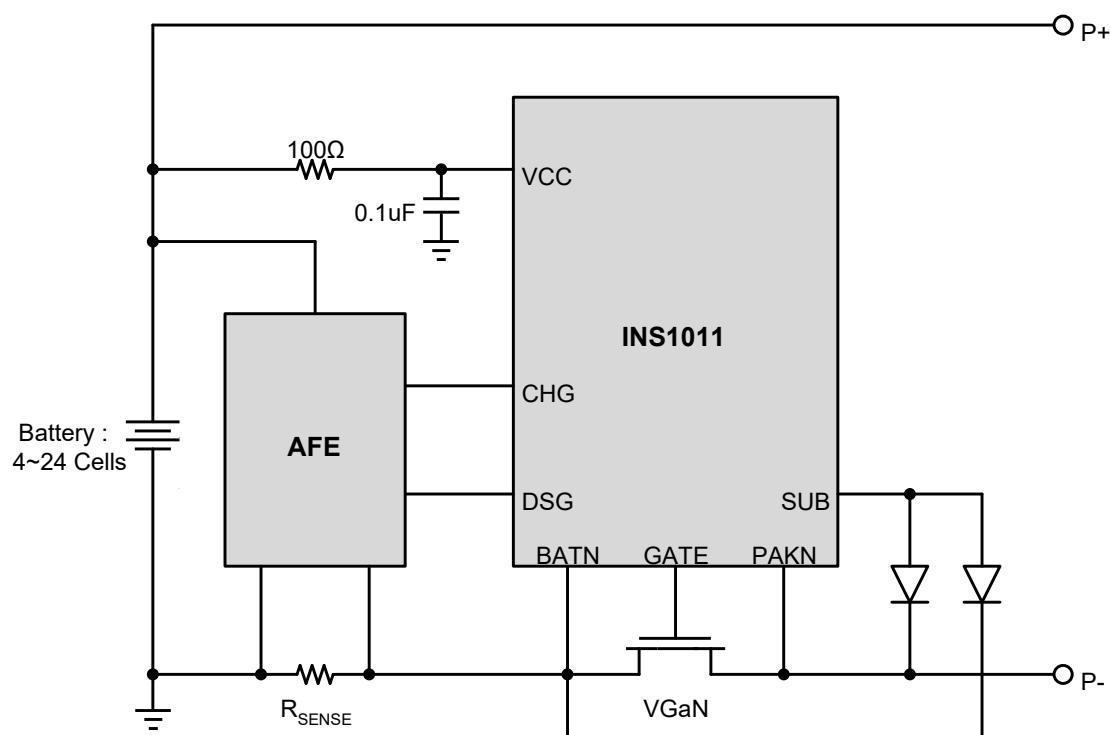


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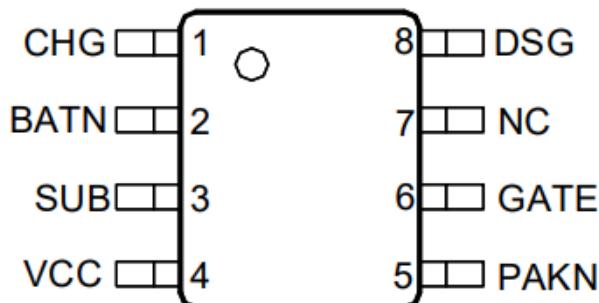
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5. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2025-03-10	Final datasheet release

6. Pin Configuration and Functions



8-Lead SOP Package – Top View

Pin Number	Pin Name	Description
1	CHG	Charging Command Input. Receive signal from external AFE or MCU and be compatible with back-to-back MOSFET driving signals.
2	BATN	Battery Negative Terminal. All power and signal inputs are referenced to this pin as ground connection.
3	SUB	Internal Substrate of the Chip.
4	VCC	Power Supply. This pin supplies the whole chip and must be locally based with a ceramic capacitor.
5	PAKN	Pack Negative Terminal.
6	GATE	Gate Driver Output. Connect this pin to the Gate of V _G N HEMT.
7	NC	No Internal Connection.
8	DSG	Discharging Command Input. Receive signal from external AFE or MCU and be compatible with back-to-back MOSFET driving signals.

7. Absolute Maximum Ratings

All pins are referenced to BATN pin, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device lifetime.

Parameter	Min	Max	Unit
VCC Voltage	-0.3	110	V
GATE Voltage	-60	6	V
PAKN Voltage	-60	130	V
SUB Voltage	-60	0.7	V
CHG , DSG Voltage, Continuous	-0.3	20	V
CHG , DSG Voltage, Transient ⁽¹⁾	-1	20	V
Operating Junction Temperature T _J	-55	150	°C
Storage Temperature	-55	150	°C

(1) Intended for repetitive events, t_{PULSE}<100ns

8. ESD Ratings

Parameter	Value	Unit
Human Body Model (HBM)	±500	V
Charged Device Model (CDM)	±1000	V

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
VCC Voltage	8	90	V
(VCC – PAKN) Voltage	0	100	V
PAKN Voltage	-59	120	V
CHG , DSG Voltage	0	15	V
Operating Junction Temperature T _J	-40	125	°C

10. Thermal Information

Symbol	Parameter	INS1011SD	Unit
R _{θJA}	Thermal Resistance, Junction to Ambient	132.95	°C/W
R _{θJC}	Thermal Resistance, Junction to Case	75.98	°C/W

According to standards defined in JESD51 and JESD51-1, thermal characteristics of the package are simulated. R_{θJA} is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

11. Electrical Characteristics

$T_J = 25^\circ\text{C}$, $VCC = 48\text{V}$, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
VCC Supply						
VCC quiescent current	I_{CC_Q}		8 9 10	13 13 15	uA	CHG = 0V, DSG = 0V, VCC=48V CHG = 0V, DSG = 5V, VCC=48V CHG = 5V, DSG = 0V, VCC=48V
VCC operating current	I_{CC_OP}			20	uA	CHG = 5V, DSG = 5V
CHG/DSG Inputs						
Input high threshold	V_{INH}		2.5	3	V	
Input low threshold	V_{INL}	1.3	1.8		V	
Input hysteresis	V_{IN_HYS}		0.7		V	
Input pulldown resistance	R_{IN}		2		MΩ	
Gate Driver						
Gate voltage – (GATE-BATN)	$V_{GATE-BATN}$	4.8	5.0	5.2	V	CHG = 5V, DSG = 5V
Gate voltage – (GATE-BATN)	$V_{GATE-BATN}$			0.05	V	CHG = 5V, DSG = 0V
Gate voltage – (GATE-PAKN)	$V_{GATE-PAKN}$			0.05	V	CHG = 0V, DSG = 5V
Gate peak source current	I_{GATE_SOR}		5		mA	
Gate peak sink current	I_{GATE_SNK}		20		mA	
Intelligent Gate Selection						
PAKN rising threshold	V_{PAKN+}		0.15		V	CHG = 0V, DSG = 0V
PAKN falling threshold	V_{PAKN-}		-0.15		V	CHG = 0V, DSG = 0V

12. Switching Characteristics

$T_J = 25^\circ\text{C}$, $VCC = 48\text{V}$, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Turn-on propagation delay ⁽²⁾	t_{PD_ON}		4		us	$C_{load}=50\text{nF}$, $BATN=PAKN=0$
Turn-off propagation delay ⁽²⁾	t_{PD_OFF-}		1		us	$C_{load}=50\text{nF}$, $BATN=PAKN=0$
Gate rise time ⁽²⁾	t_R		70		us	$C_{load}=50\text{nF}$, 10% to 90%
Gate fall time ⁽²⁾	t_F		30		us	$C_{load}=50\text{nF}$, 90% to 10%

(2) Not 100% tested and guaranteed by design.

13. Typical Characteristics

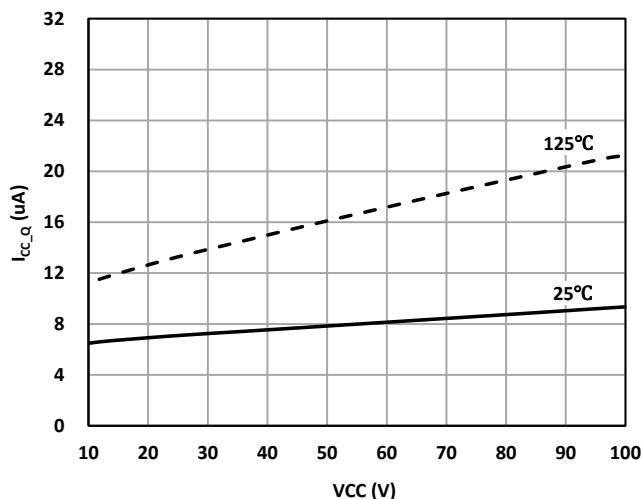


Figure 1. VCC Quiescent Current vs VCC

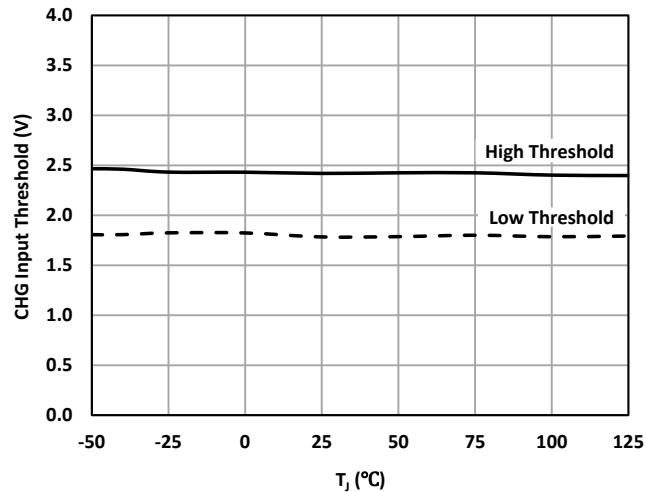


Figure 2. CHG Input Threshold VS Temperature

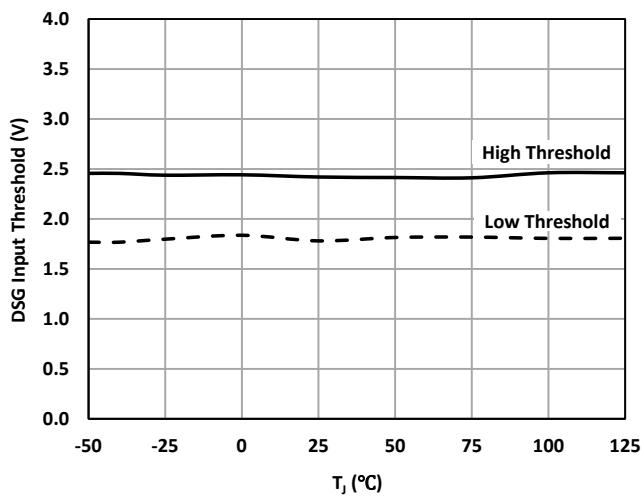


Figure 3. DSG Input Threshold VS Temperature

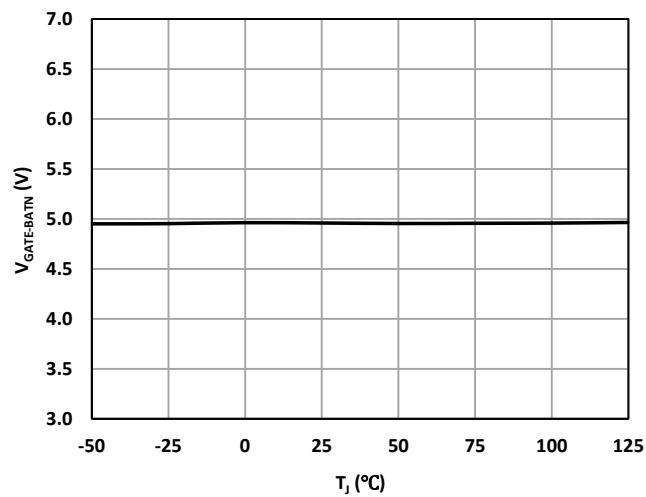


Figure 4. Gate Voltage VS Temperature

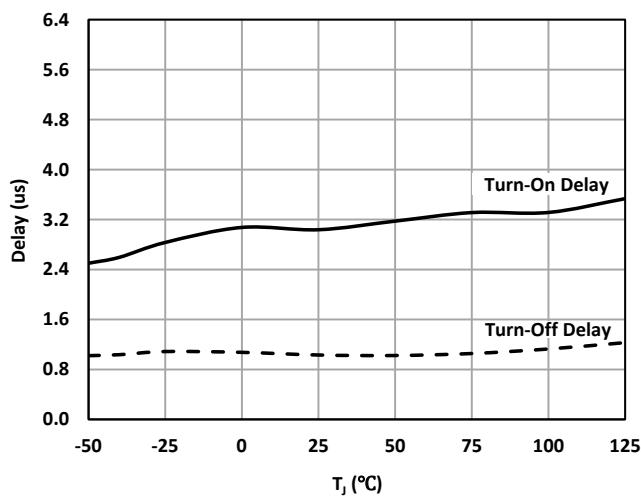


Figure 5. Propagation Delay VS Temperature

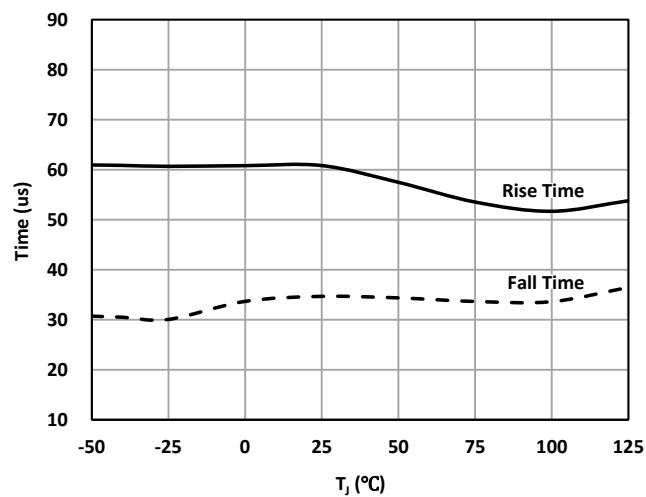


Figure 6. Gate Rise/Fall Time VS Temperature

14. Block Diagram

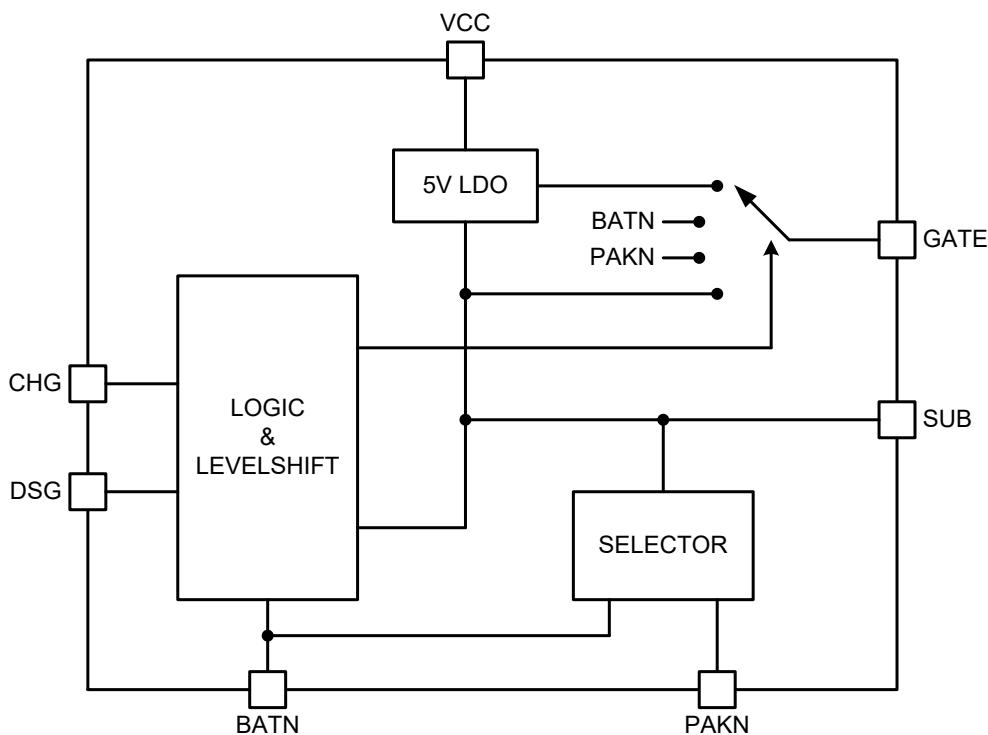


Figure 7. Functional Block Diagram

15. Function Description

INS1011 is a driver of E-mode Bi-directional GaN HMET with Single Gate (VGaN) for low-side battery protection in BMS system. The device is compatible with AFE or battery MCU, which provides independent control charge and discharge of a battery pack, allowing the battery monitor device or battery MCU to always maintain communication to the host system regardless if the protection FETs are on or off.

Supply Voltage

The INS1011 can be connected directly to a battery stack, up to 90V battery voltage.

Input Configuration

The INS1011 allows independent control on charging and discharge via the CHG/DSG pins. The device has internal charging and discharging control pin CHG, DSG to control the Gate driver output. The CHG and DSG inputs can be connected to low-side FET driver outputs of an Analog Front End (AFE), a general purpose microcontroller, or dedicated battery pack controller. Figure 8 illustrates the timing diagram of the input CHG/DSG and the output GATE.

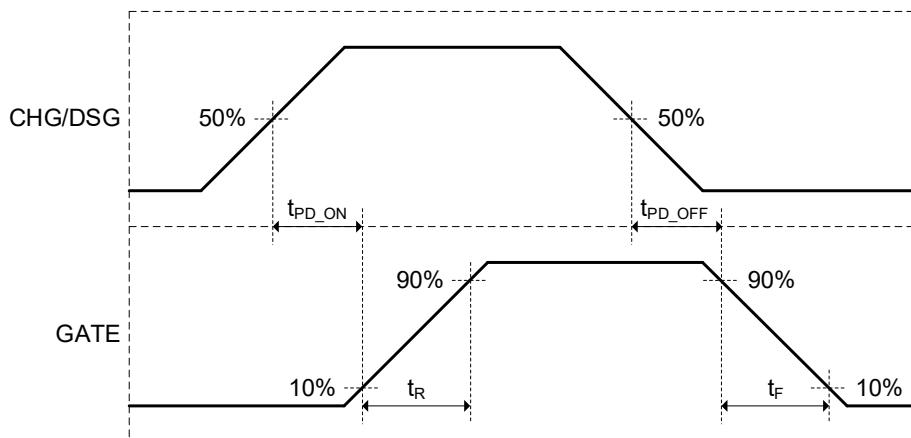


Figure 8. Timing Diagram

Driver Output

The device drive output pin Gate to control external single gate bi-direction E-mode GaN HEMT (V_{GaN}) ON/OFF. The typical driver voltage is around 5V, which is clamped below 6V for the Gate reliability of V_{GaN} HEMT.

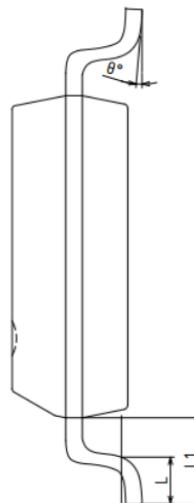
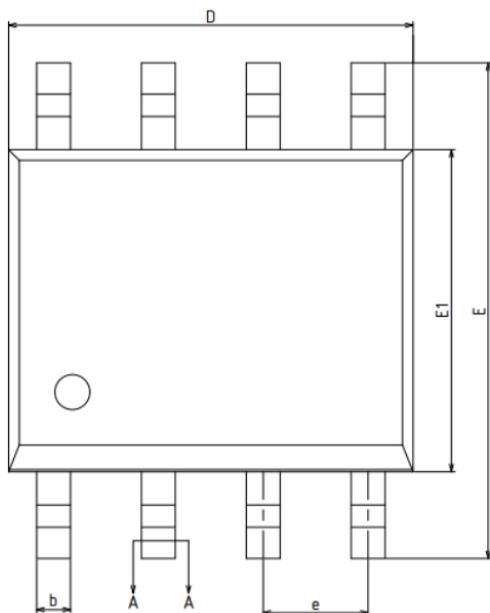
State Truth Table

The state truth table lists all valid combinations for the two control pins (CHG and DSG), along with the corresponding protection mode of each pin combination. In OFF Protection Mode, the INS1011 device monitors the input voltages from PAKN and BATN, transitioning to whichever GATE connection it is commanded to.

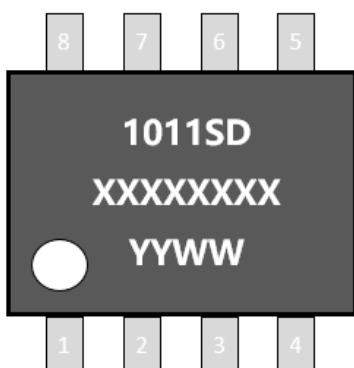
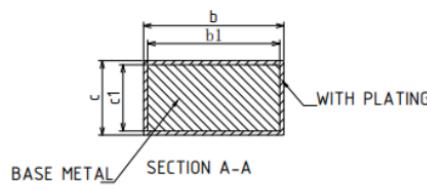
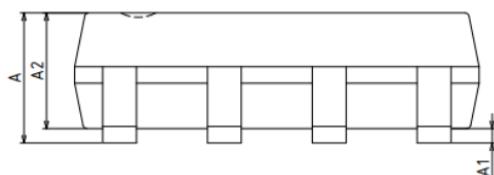
CHG	DSG	GATE Connection	Mode	Condition
0	0	BATN	OFF Protection	$V_{PAKN} > V_{BATN}$
0	0	PAKN	OFF Protection	$V_{PAKN} < V_{BATN}$
0	1	PAKN	Charge Protection	
1	0	BATN	Discharge Protection	
1	1	5V	ON	

16. Package Information

SOP8 Package:

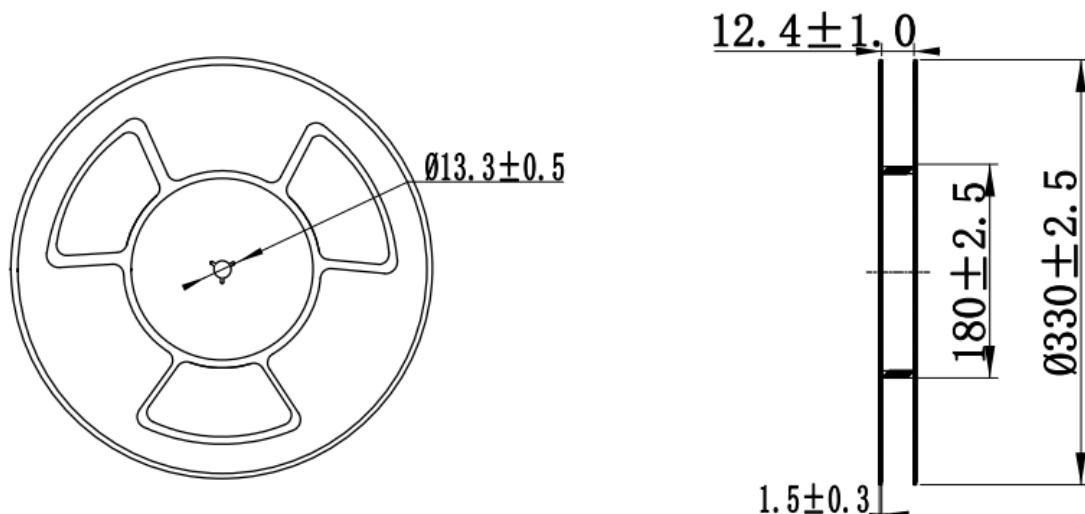
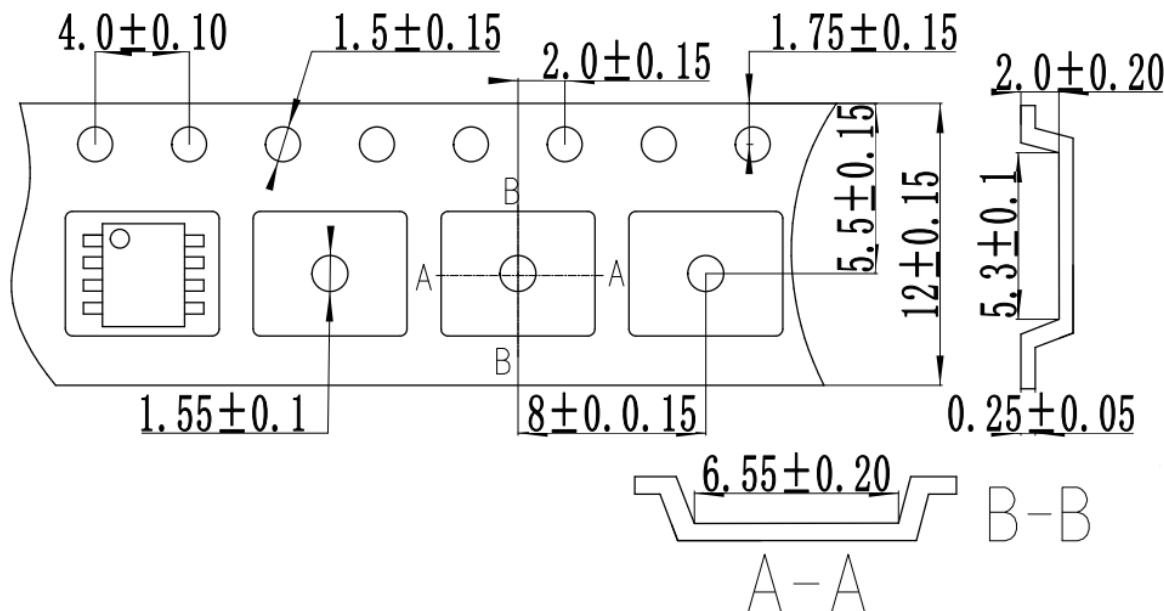


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.75
A1	0.10	-	0.25
A2	1.30	1.40	1.50
b	0.31	-	0.50
b1	0.30	0.40	0.45
c	0.20	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.40	-	0.80
L1		1.05REF	
θ	0	-	8°

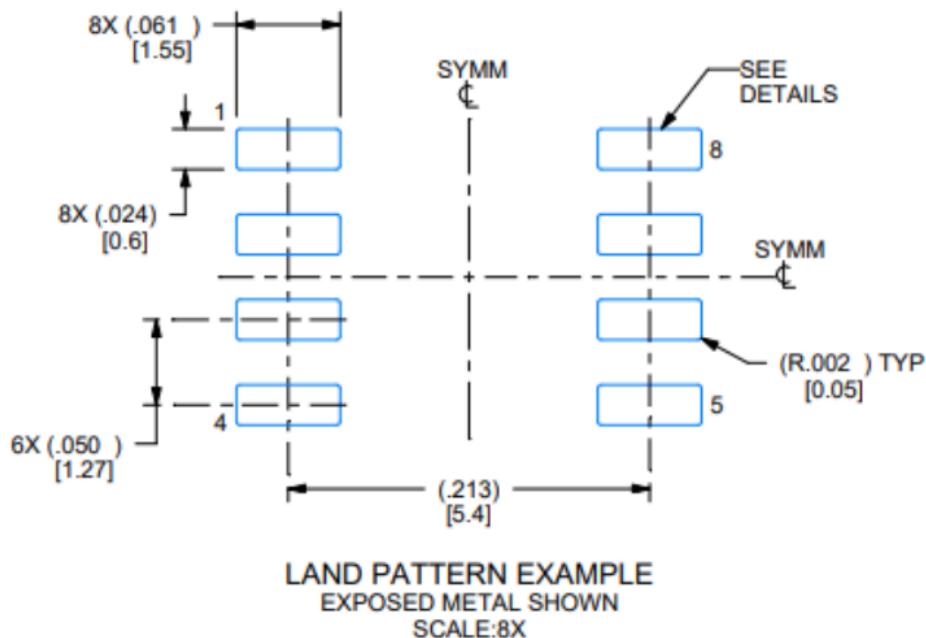


Row	Description	Example
Row1	Product Name(In short)	1011SD
Row2	ASSY lot No.	XXXXXXXX
Row3	Date code	YYWW

17. Tape and Reel Information



18. Recommended Land Pattern



19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
INS1011SD	SOP8	1011SD	MSL3	13" 3000PCS/reel

Important Notice

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