

INN700TA105C

1. General description

700V GaN-on-Silicon Enhancement-mode Power Transistor in TOLL package.

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

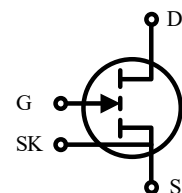
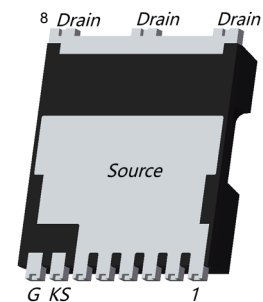
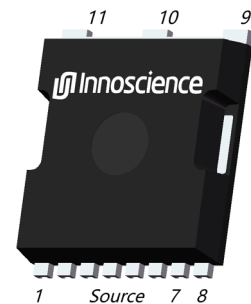
3. Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast battery charging
- High density power conversion
- High efficiency power conversion

4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	700	V
$R_{DS(on),max} @ V_{GS} = 6\text{ V}$	105	m Ω
$Q_{G,typ} @ V_{DS} = 400\text{ V}$	4.8	nC
$I_{D,pulse}$	43.5	A
$Q_{OSS} @ V_{DS} = 400\text{ V}$	56	nC
$Q_{rr} @ V_{DS} = 400\text{ V}$	0	nC



5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	9, 10, 11	7	1, 2, 3, 4, 5, 6

Table 3 Ordering information

Type/Ordering Code	Package	Product Code	Carrier	Package base Qty.
INN700TA105C	TOLL	70TA105C	Tape & Reel	1200

Table of contents

1. General description1

2. Features.....1

3. Applications1

4. Key performance parameters.....1

5. Pin information.....1

6. Maximum ratings3

7. Thermal characteristics.....4

8. Electric characteristics.....5

9. Electric characteristics diagrams7

10.Package outlines.....13

11.Reel information.....14

12.Recommended PCB footprint15

13.Revision history.....16

6. Maximum ratings

at $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscience sales office

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,max}$	700	V	$V_{GS} = 0\text{ V}$, $T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Drain source voltage transient ¹	$V_{DS,transient}$	800	V	$V_{GS} = 0\text{ V}$
Drain source voltage, pulsed ²	$V_{DS,pulse}$	750	V	$T_j = 25\text{ }^{\circ}\text{C}$; total time < 10 h
				$T_j = 125\text{ }^{\circ}\text{C}$; total time < 1 h
Continuous current, drain source	I_D	21.7	A	$T_c = 25\text{ }^{\circ}\text{C}$
Pulsed current, drain source ³	$I_{D,pulse}$	43.5	A	$T_c = 25\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$; $V_{DS} = 400\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Pulsed current, drain source ³	$I_{D,pulse}$	21.7	A	$T_c = 125\text{ }^{\circ}\text{C}$; $V_G = 6\text{ V}$; $V_{DS} = 400\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Gate source voltage, continuous	V_{GS}	-6 to +7	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Gate source voltage, pulsed	$V_{GS,pulse}$	-20 to +10	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$; $t_{PULSE} = 10\text{ ns}$, $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	135.9	W	$T_c = 25\text{ }^{\circ}\text{C}$
Operating temperature	T_j	-55 to +150	$^{\circ}\text{C}$	
Storage temperature	T_{stg}	-55 to +150	$^{\circ}\text{C}$	

1 $V_{DS,transient}$ is intended for non-repetitive events, $t_{PULSE} < 200\text{ }\mu\text{s}$

2 $V_{DS,pulse}$ is intended for repetitive pulse, $t_{PULSE} < 100\text{ ns}$

3 Limit was extracted from characterization test, not measured during production

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal Resistance Junction to ambient	R_{thJA}^1	57.2	°C/W	
Thermal resistance, junction-case (bottom)	R_{thJC}	0.92	°C/W	
Maximum reflow soldering temperature	T_{sld}	260	°C	MSL3

1. R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board

8. Electric characteristics

at $T_J = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	$I_D = 24.3\text{ mA}$; $V_{DS} = V_{GS}$; $T_J = 25\text{ }^{\circ}\text{C}$
		-	1.6	-		$I_D = 24.3\text{ mA}$; $V_{DS} = V_{GS}$; $T_J = 150\text{ }^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	-	3.8	48.8	μA	$V_{DS} = 700\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$
		-	9.8	-		$V_{DS} = 700\text{ V}$; $V_{GS} = 0\text{ V}$; $T_J = 150\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	122.3	-	μA	$V_{GS} = 6\text{ V}$; $V_{DS} = 0\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$
Drain-source on-state resistance	$R_{DS(on)}$	-	80	105	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 6\text{ A}$; $T_J = 25\text{ }^{\circ}\text{C}$
		-	180	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 6\text{ A}$; $T_J = 150\text{ }^{\circ}\text{C}$
Gate resistance	R_G	-	2.3	-	Ω	$f = 5\text{ MHz}$; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	179	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	66.2	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Reverse transfer Capacitance	C_{rss}	-	0.7	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	102	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	140	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	56	-	nC	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$

- $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V
- $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	4.8	-	nC	$V_{GS} = 0 \text{ to } 6 \text{ V}; V_{DS} = 400 \text{ V};$ $I_D = 6 \text{ A}$
Gate-source charge	Q_{GS}	-	0.4	-	nC	
Gate-drain charge	Q_{GD}	-	2.2	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.2	-	V	$V_{DS} = 400 \text{ V}; I_D = 6 \text{ A}$

Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.6	-	V	$V_{GS} = 0 \text{ V}; I_S = 6 \text{ A}$
Pulsed current, reverse	$I_{S,pulse}$	-	-	43.5	A	$V_{GS} = 6 \text{ V}; t_{PULSE} = 10 \mu\text{s}$
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_{SD} = 6 \text{ A}; V_{SD} = 400 \text{ V}$
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

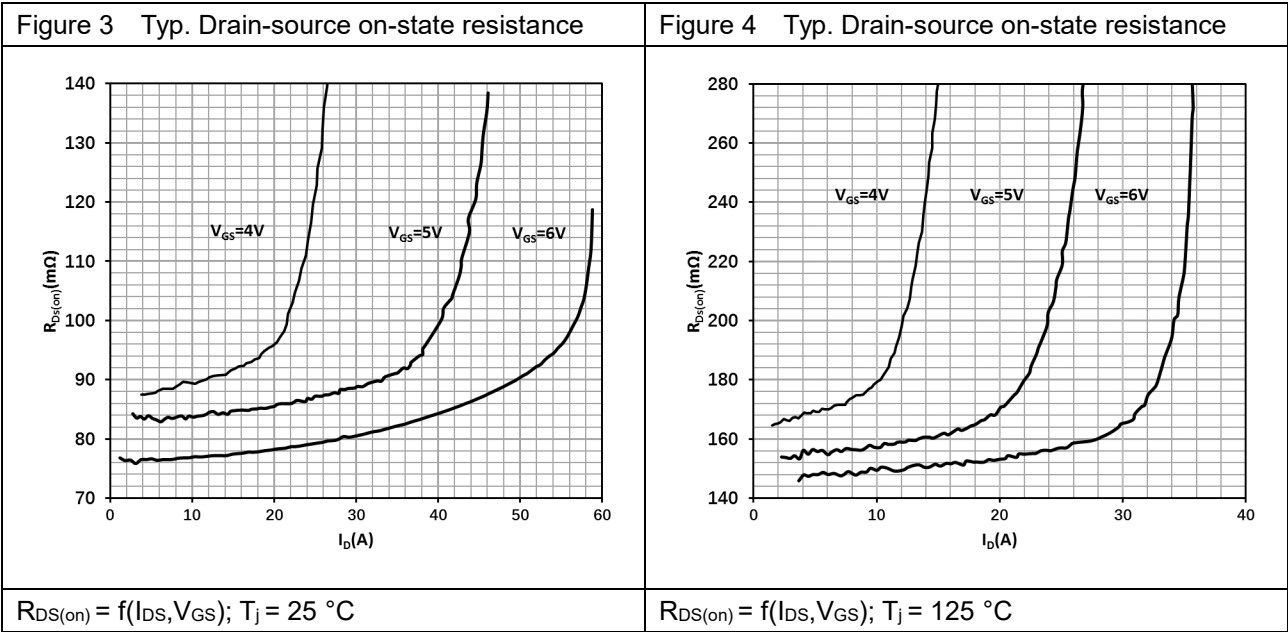
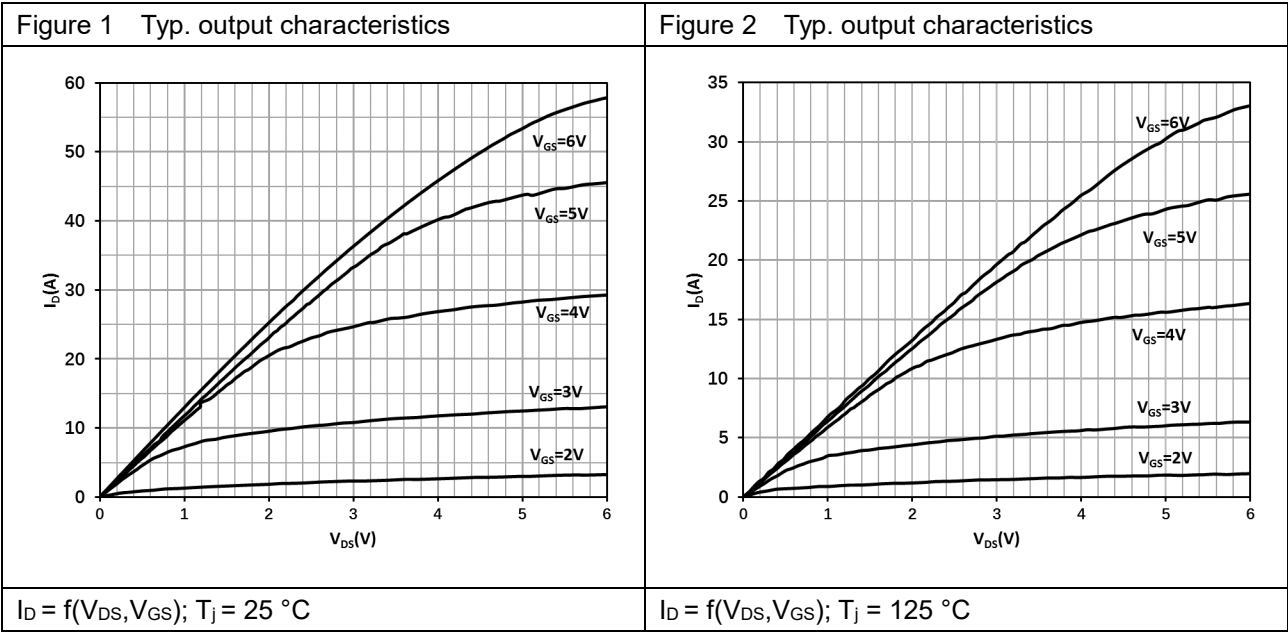
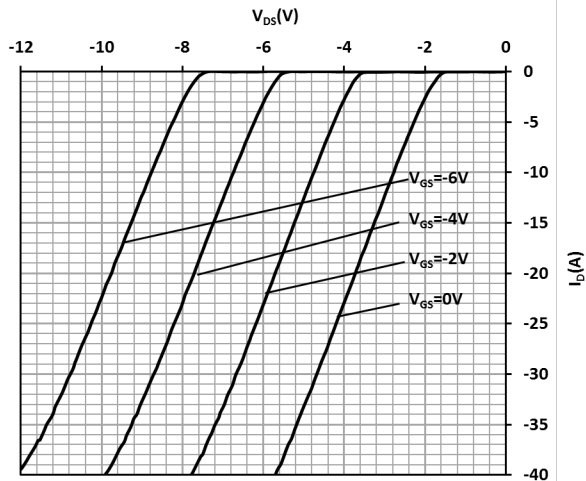
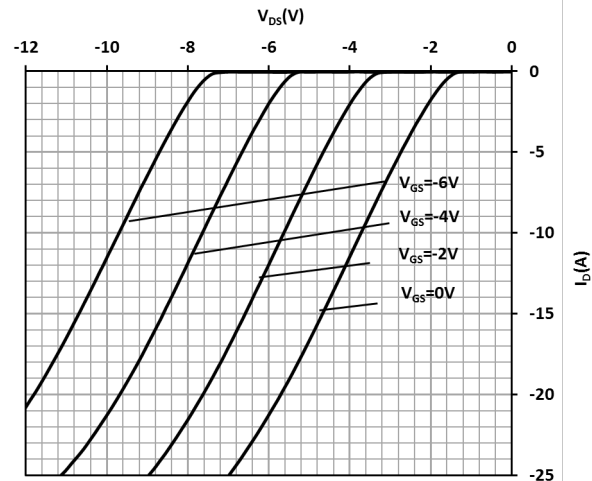


Figure 5 Typ. channel reverse characteristics



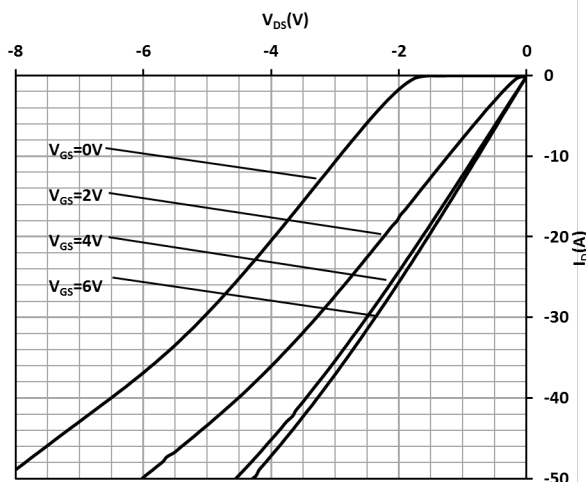
$$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^{\circ}\text{C}$$

Figure 6 Typ. channel reverse characteristics



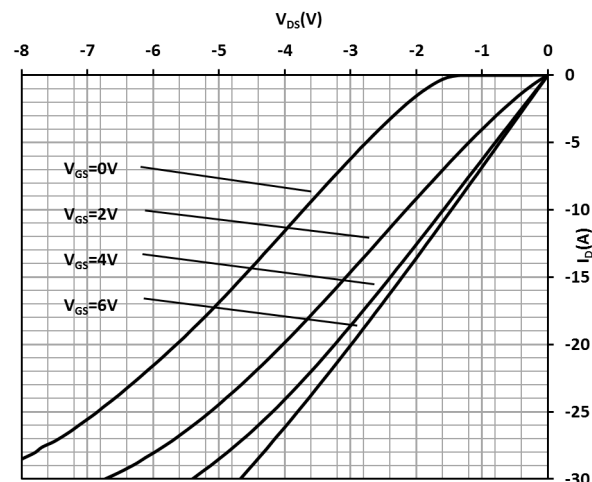
$$I_D = f(V_{DS}, V_{GS}); T_J = 125\text{ }^{\circ}\text{C}$$

Figure 7 Typ. channel reverse characteristics



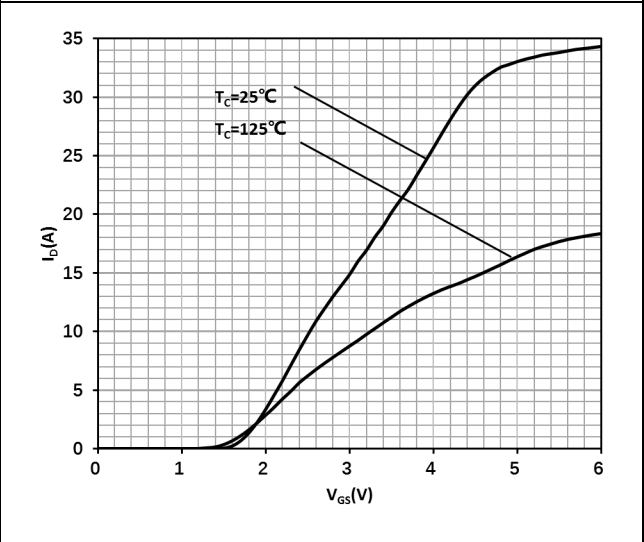
$$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^{\circ}\text{C}$$

Figure 8 Typ. channel reverse characteristics



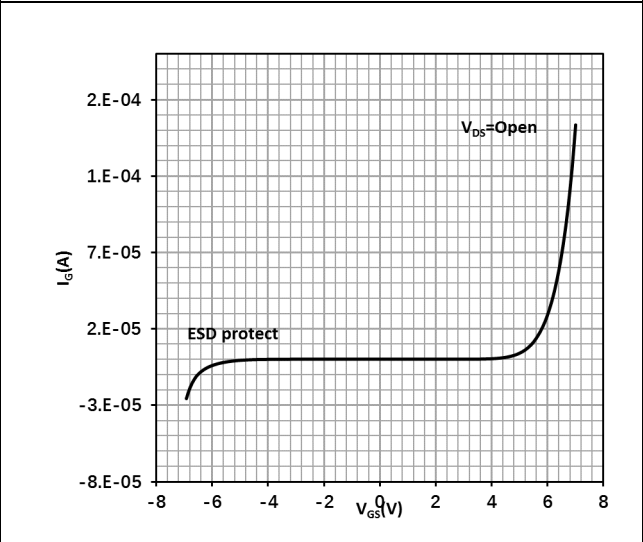
$$I_D = f(V_{DS}, V_{GS}); T_J = 125\text{ }^{\circ}\text{C}$$

Figure 9 Typ. transfer characteristics



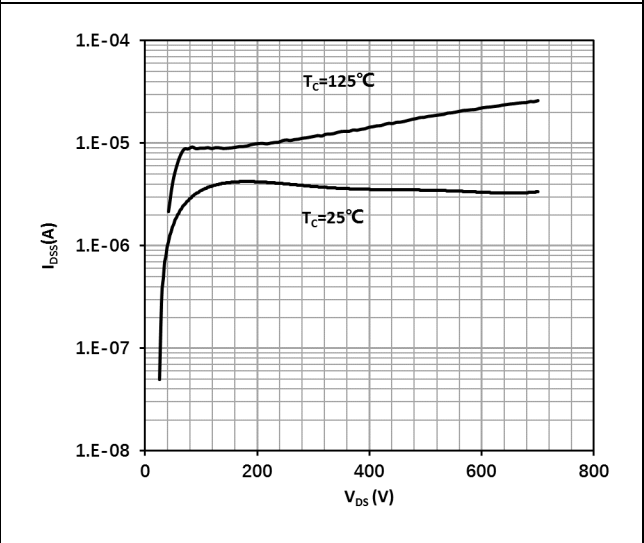
$I_D = f(V_{GS}); V_{DS} = 3\text{ V}$

Figure 10 Typ. Gate-to-Source leakage



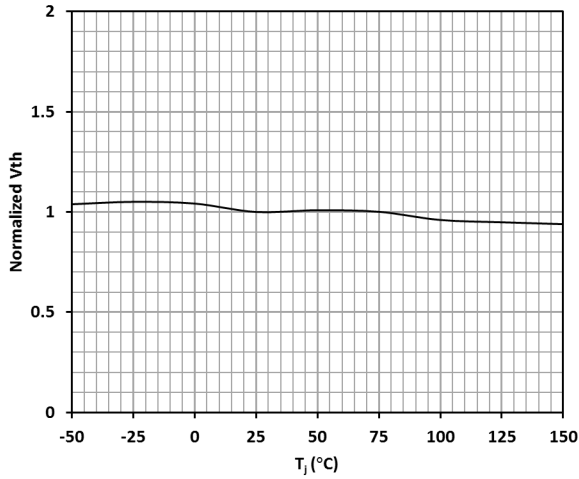
$I_G = f(V_{GS}); I_G$ reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



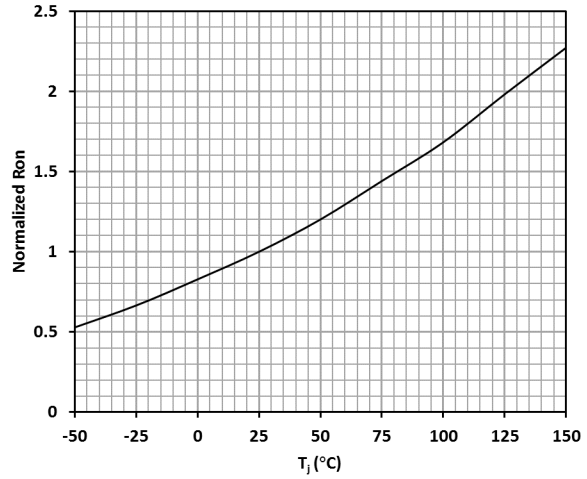
$I_{DSS} = f(V_{DS}); V_{GS} = 0\text{ V}$

Figure 12 Gate threshold voltage



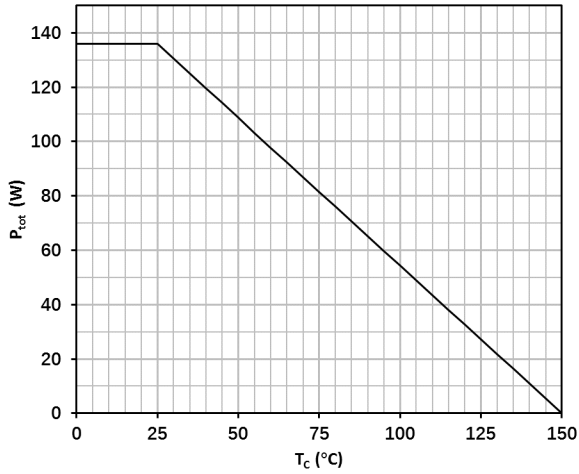
$$V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 24.3 \text{ mA}$$

Figure 13 Drain-source on-state resistance



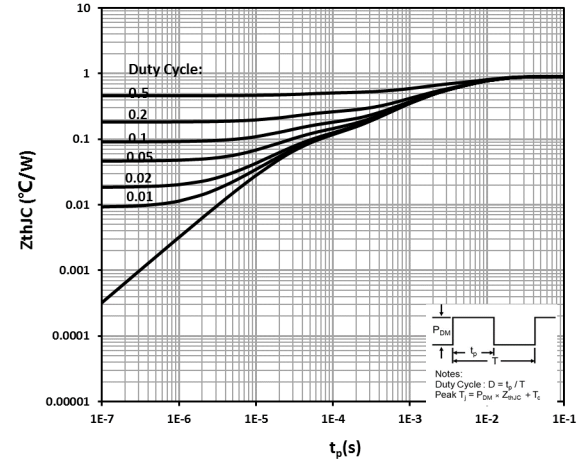
$$R_{DS(on)} = f(T_j); I_D = 6 \text{ A}; V_{GS} = 6 \text{ V}$$

Figure 14 Power dissipation



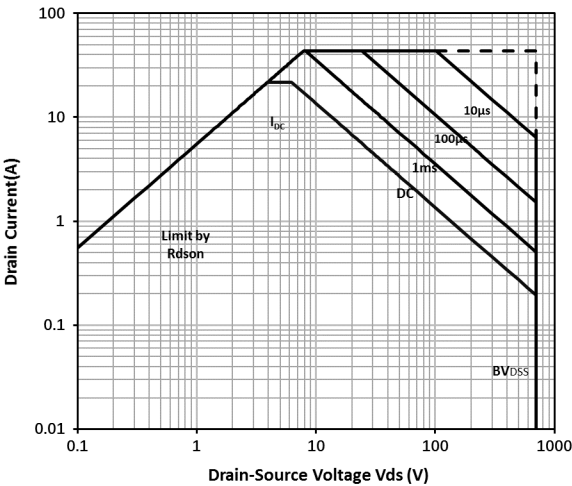
$$P_{tot} = f(T_c)$$

Figure 15 Max.transient thermal impedance



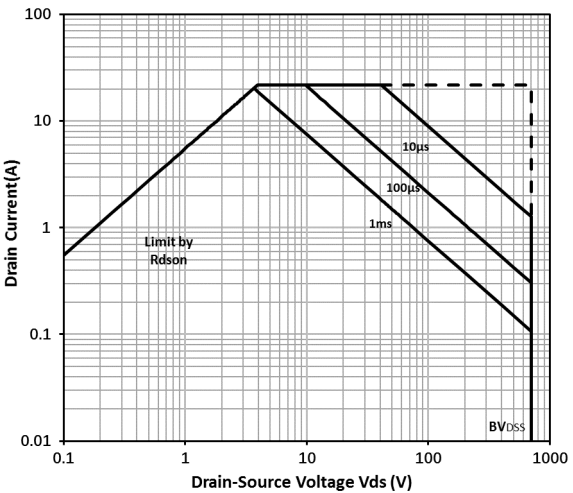
$$Z_{thJC} = f(t_p, D)$$

Figure 16 Safe operating area



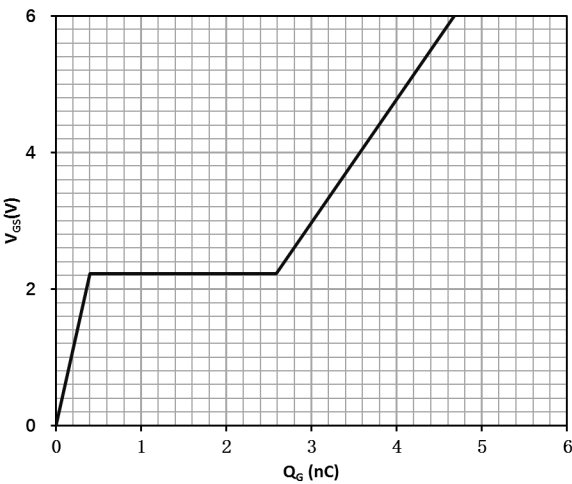
$$I_D = f(V_{DS}); T_C = 25\text{ }^{\circ}\text{C}$$

Figure 17 Safe operating area



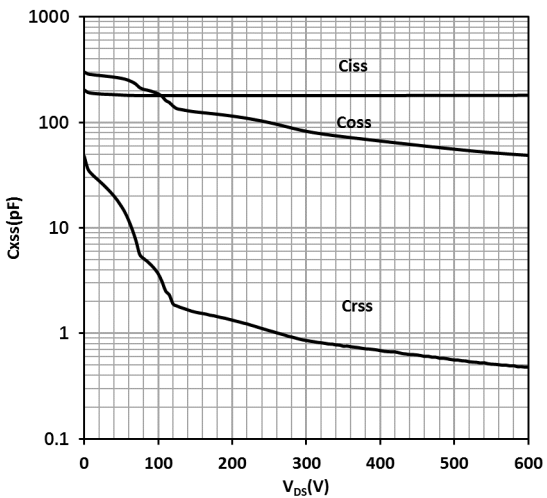
$$I_D = f(V_{DS}); T_C = 125\text{ }^{\circ}\text{C}$$

Figure 18 Typ. gate charge



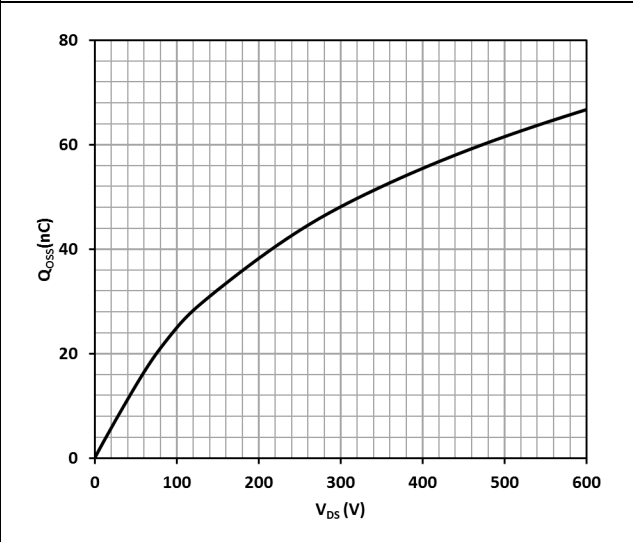
$$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 6\text{ A}$$

Figure 19 Typ. capacitances



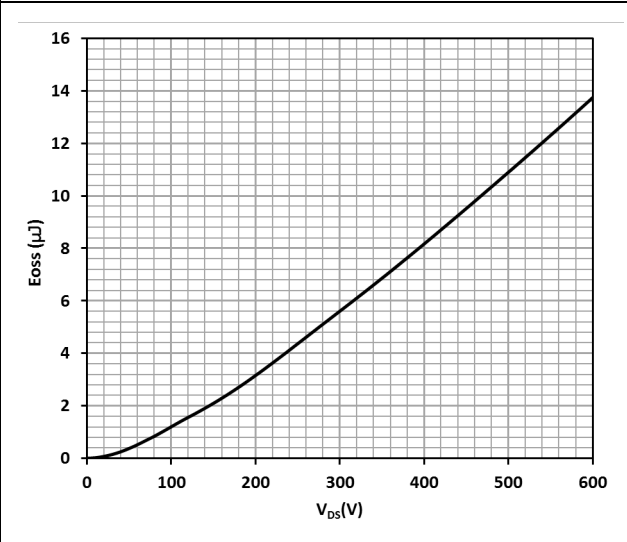
$$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$$

Figure 20 Typ. output charge



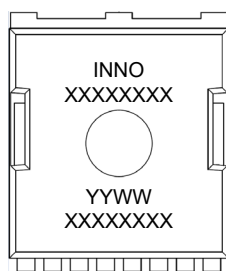
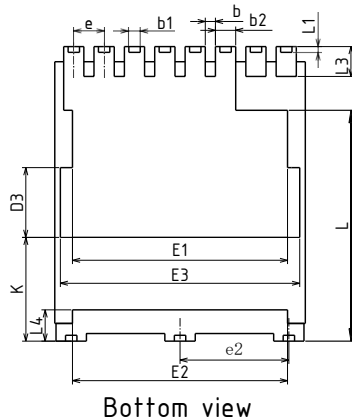
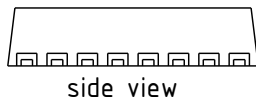
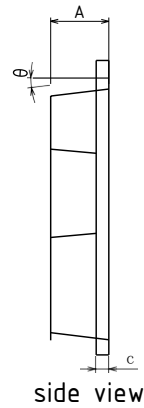
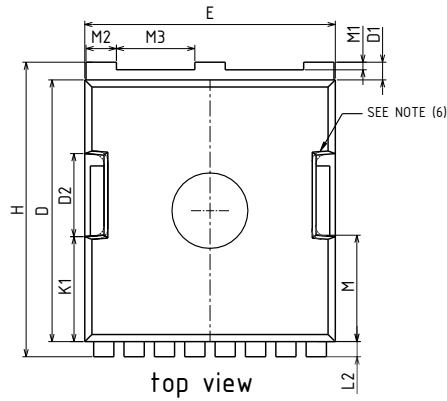
$Q_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 21 Typ. C_{oss} stored Energy



$E_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

10. Package outlines

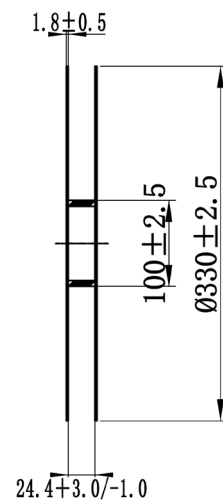
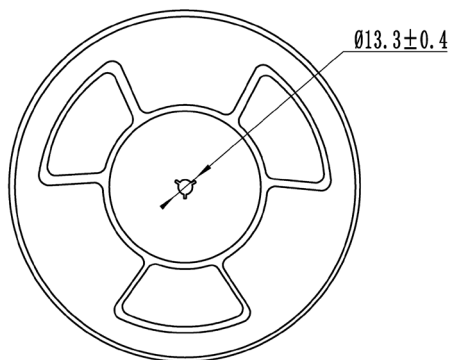
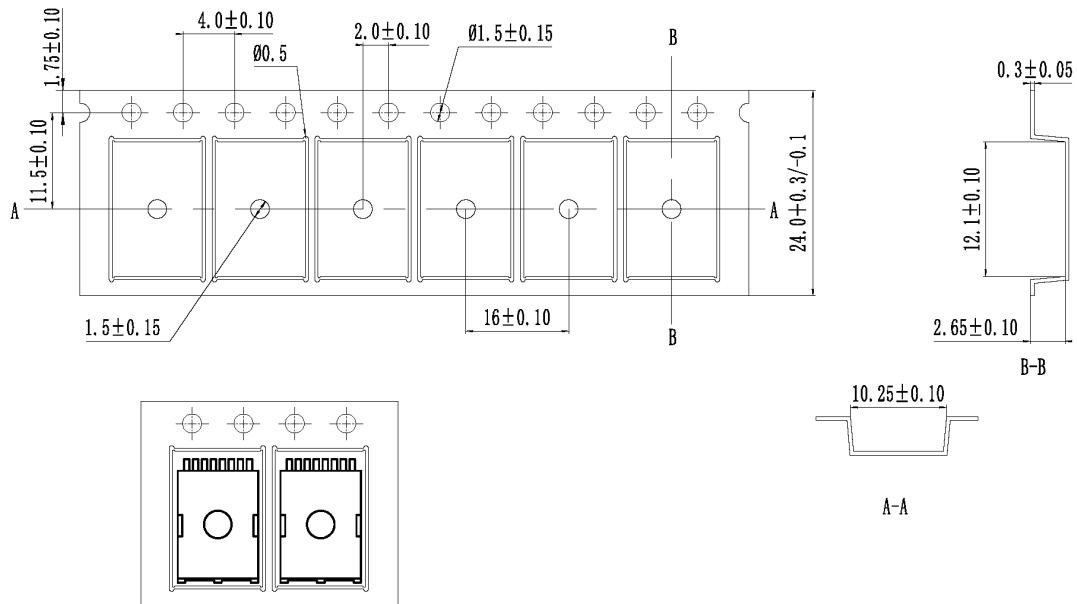


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.15	2.30	2.45
b	0.30	0.40	0.50
b1	0.31	0.43	0.55
b2	0.65	0.80	0.90
c	0.40	0.50	0.60
D	10.18	10.38	10.58
D1	0.50	0.70	0.90
D2	3.30REF		
D3	2.77REF		
E	9.70	9.90	10.10
E1	8.50REF		
E2	8.50REF		
E3	9.46REF		
e	1.10	1.20	1.30
e2	4.20	4.30	4.40
H	11.48	11.68	11.88
K	4.08REF		
K1	4.18REF		
L	9.13REF		
L1	0.23REF		
L2	0.50	0.60	0.70
L3	1.00	1.20	1.40
L4	1.00	1.20	1.40
M	4.18REF		
M1	0.26REF		
M2	1.10	1.20	1.30
M3	3.10REF		
Θ	10.00REF		

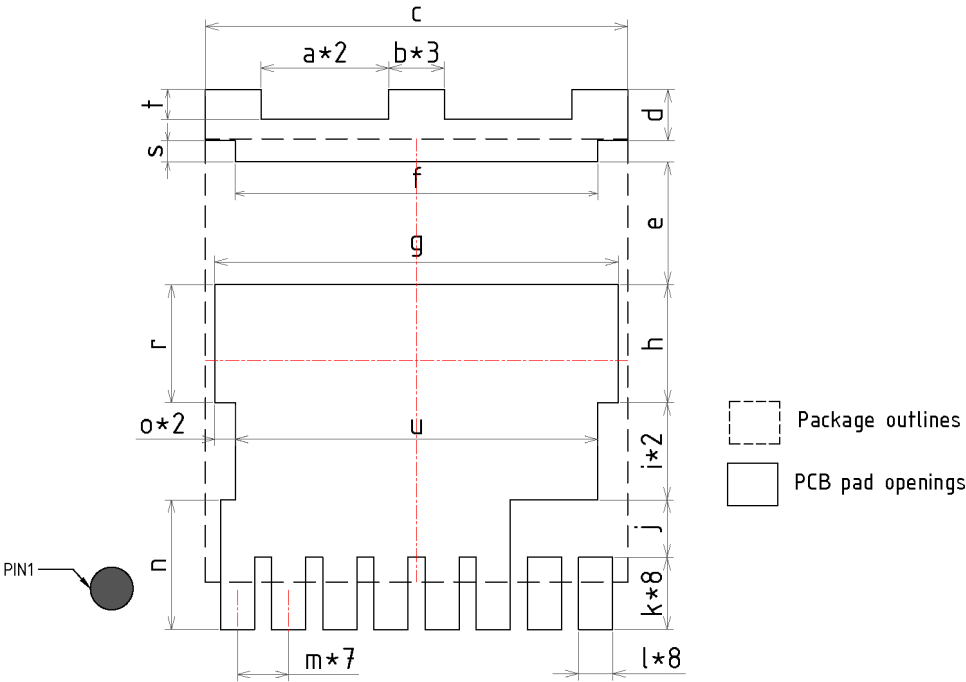
Row	Description	Example
Row1	Company name	INNO
Row2	Product code (In short)	XXXXXXXXX
Row3	Date code	YYWW
Row4	ASSY lot No.	XXXXXXXXX

- (1) Dimensioning and tolerancing confirm to ASME Y14.5M-1994
- (2) All dimensions are in millimeters, angles are in degrees
- (3) Coplanarity applies to the exposed heat slug as well as the terminal
- (4) Radius on terminal is optional
- (5) General tolerance: ± 0.10 mm
- (6) Supplier dependent mold cavity , filleted corners or square corners

11. Reel information



12. Recommended PCB footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	3.00	k	1.70
b	1.30	l	0.80
c	9.90	m	1.20
d	1.20	n	3.05
e	2.88	o	0.48
f	8.50	r	2.77
g	9.46	s	0.50
h	2.77	t	0.70
i	2.28	u	8.50
j	1.35	/	/

Notes:
 (1) All dimension are in millimeters.
 (2) Drawing is not to scale.

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-07-05	1.0 version release
1.1	2025-07-11	Update Ordering, Package outlines and PCB footprint information.

Important Notice

The information provided in this document is intended as a guide only and shall not in any event be regarded as a guarantee of conditions, characteristics or performance. Innoscience does not assume any liability arising out of the application or use of any product described herein, including but not limited to any personal injury, death, or property or environmental damage. No licenses, patent rights, or any other intellectual property rights is granted or conveyed. Innoscience reserves the right to modify without notice. All rights reserved.