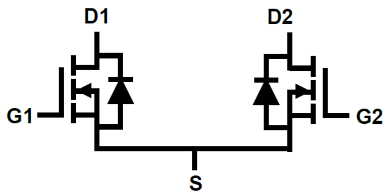
INN100W14

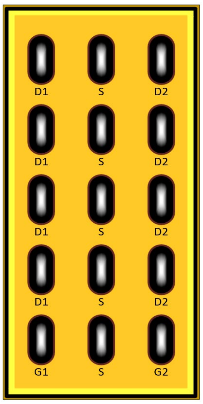
General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) with ultra-low on resistance.



Features

- GaN-on-Silicon E-mode HEMT technology
- Dual Channels, Common Source
- Ultra High Switching Frequency
- Fast and Controllable Fall and Rise Time
- Ultra-low on Resistance



Package: WLCSP 5X3
Size: 1.58mmX3.58mm

Applications

- Point of Load Converters
- Lidar Application
- Class-D Audio
- Envelope Tracking Power Supplies
- Pulsed Power Applications

Maximum ratings (Q1 & Q2)

Symbol	Parameter	Max	Unit
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
I_D	Continuous Current	7	A
	Pulsed (25˚C, T_{Pulse} = 100 µs)	90	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.5	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	5.0	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	62	˚C/W

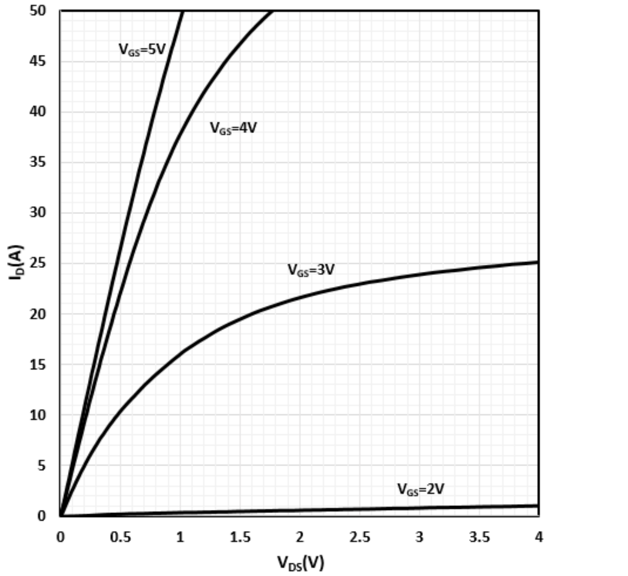
Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

Electrical Characteristics (TJ =25°C unless otherwise stated) (Q1 & Q2)

Symbol	Parameter	Min	Typ.	Max	Unit	Test Condition
Static Parameters						
BV_{DSS}	Drain-to-Source Voltage	100			V	V_{GS} = 0 V, I_D = 120μA
I_{DSS}	Drain Source Leakage		20	80	μA	V_{GS} = 0 V, V_{DS} = 80V
I_{GSS}	Gate-to-Source Forward Leakage		0.1	1	mA	V_{GS} = 5 V
	Gate-to-Source Reverse Leakage		20	80	μA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.3	2.4	V	V_{DS} = V_{GS}, I_D = 1.9mA
$R_{DS(on)}$	Drain-Source On Resistance		19	25	mΩ	V_{GS} = 5 V, I_D = 7A
V_{SD}	Source-Drain Forward Voltage		1.9		V	I_S = 0.8 A, V_{GS} = 0 V
Dynamic Parameters						
C_{iss}	Input Capacitance		307	384	pF	V_{GS} = 0 V, V_{DS} = 50V
C_{oss}	Output Capacitance		150	218		V_{GS} = 0 V, V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance		1.8	2.5		V_{GS} = 0 V, V_{DS} = 50V
$C_{oss(er)}$	Energy Related Coss		196			V_{GS} = 0 V, V_{DS} = 50V
$C_{oss(tr)}$	Time Related Coss		264			V_{GS} = 0 V, V_{DS} = 50V
R_G	Gate Resistance		900		mΩ	
Q_G	Total Gate Charge		2.75	3.45	nC	V_{GS} = 5V, V_{DS} = 50V, I_D=7A
Q_{GS}	Gate to Source Charge		0.65			V_{DS} = 50V,I_D=7A
Q_{GD}	Gate to Drain Charge		0.50	1.00		V_{DS} = 50V,I_D=7A
$Q_{G(TH)}$	Gate Charge at Threshold		0.40			V_{DS} = 50V,I_D=7A
Q_{OSS}	Output Charge		13.5	18.5		V_{DS} = 50V,I_D=7A

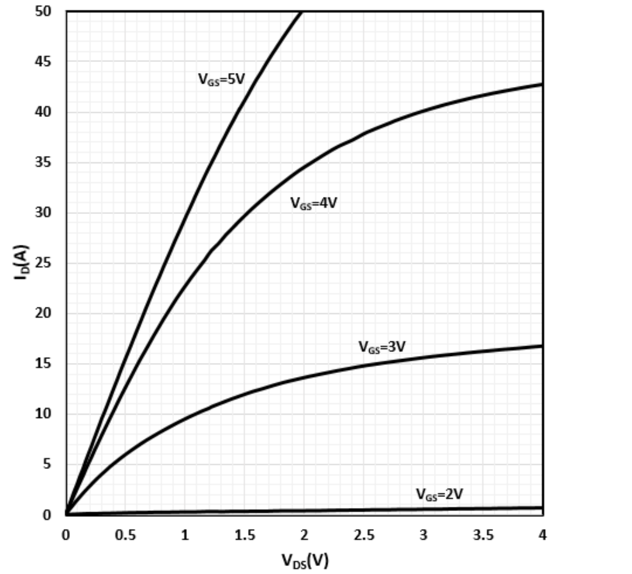
Electric characteristics diagrams

Fig1 Typ. Output Characteristics (Q1 & Q2)



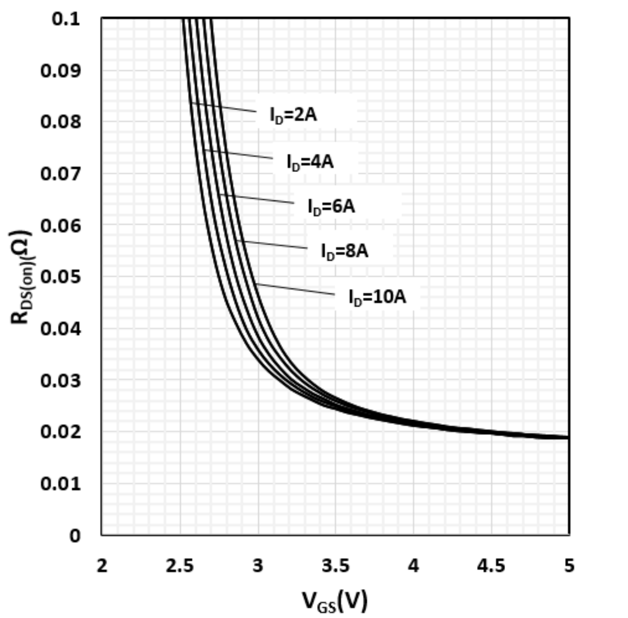
$I_D=f(V_{DS},V_{GS})$; T_J =25˚C

Fig2 Typ. Output Characteristics (Q1 & Q2)



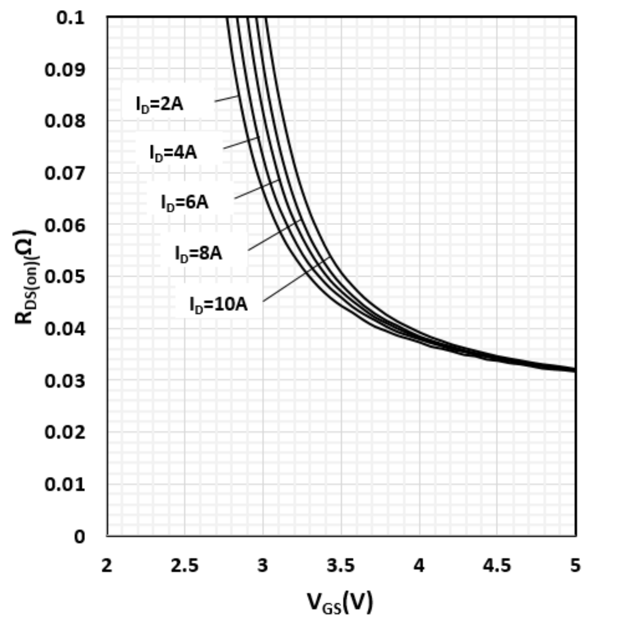
$I_D=f(V_{DS},V_{GS})$; T_J =125˚C

Fig3 Typ. Drain-Source On Resistance (Q1 & Q2)



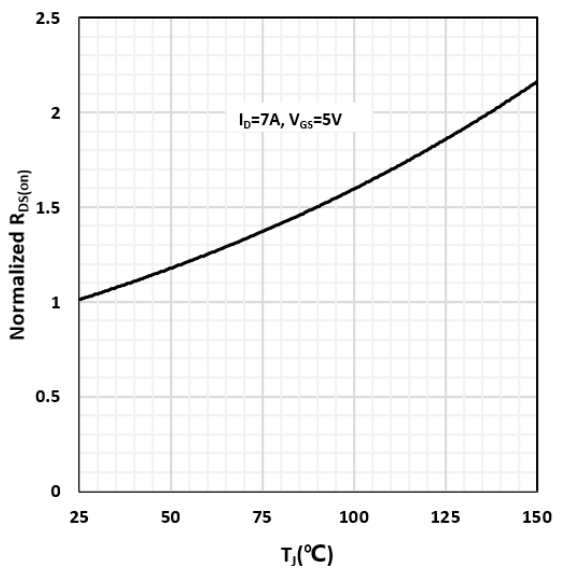
$R_{DS(on)}=f(I_D,V_{GS})$; T_J =25˚C

Fig4 Typ. Drain-Source On Resistance (Q1 & Q2)



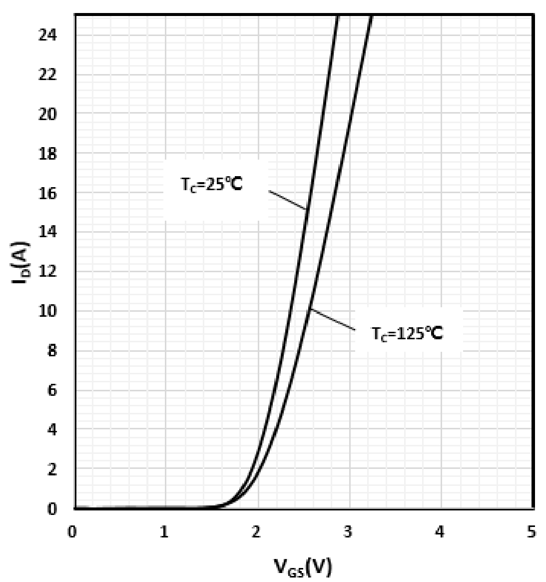
$R_{DS(on)}=f(I_D,V_{GS})$; T_J =125˚C

Fig5 On Resistance vs Temp. (Q1 & Q2)



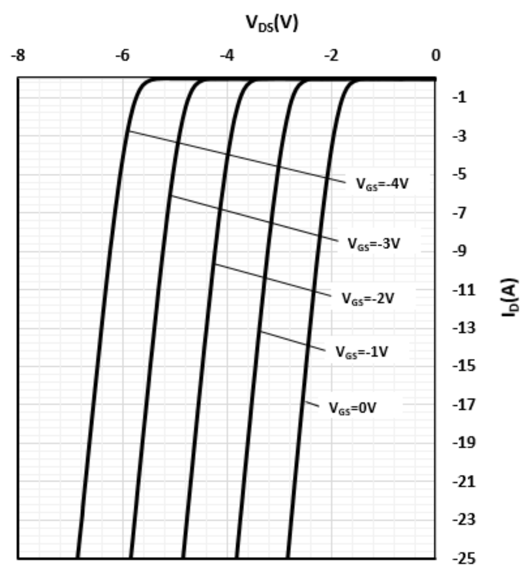
Normalized R $_{DS(on)}$=f(T_J); I_D=7A

Fig6 Typ. Transfer Characteristics (Q1 & Q2)



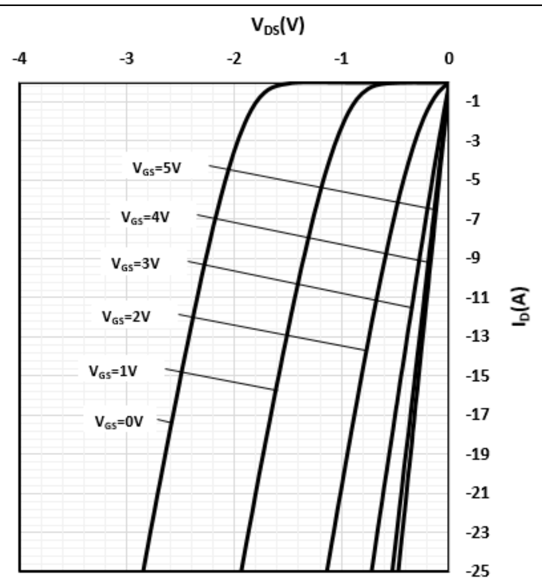
I_D=f(V_{GS}); V_{DS}=3V

Fig7 Typ. Reverse Characteristics (Q1 & Q2)



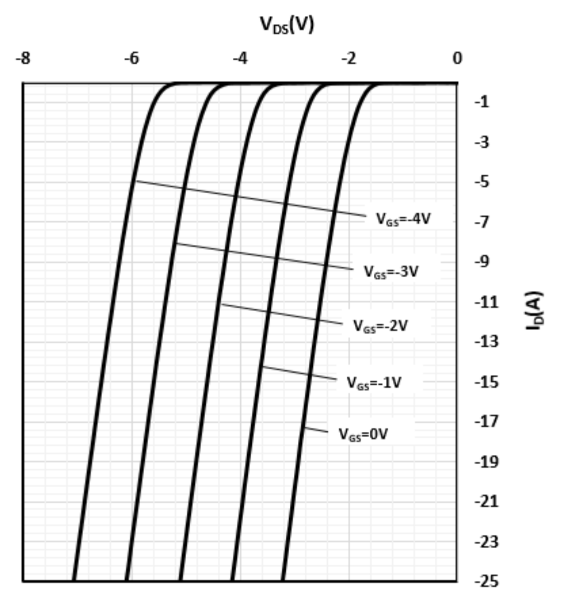
I_D=f(V_{DS},V_{GS}); T_J=25˚C

Fig8 Typ. Reverse Characteristics (Q1 & Q2)



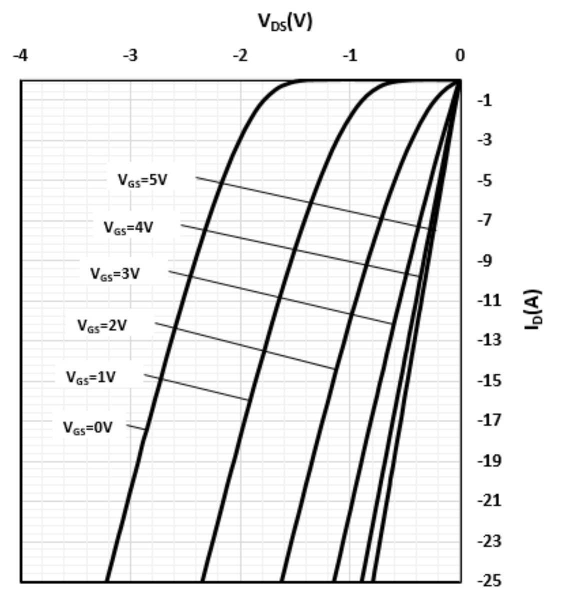
I_D=f(V_{DS},V_{GS}); T_J=25˚C

Fig9 Typ. Reverse Characteristics (Q1 & Q2)



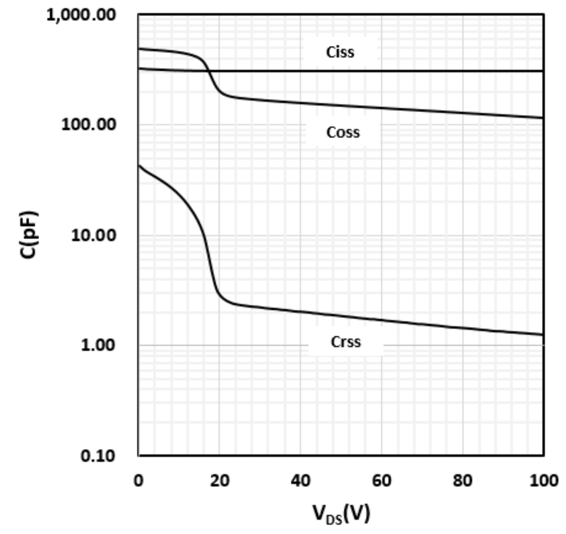
I_D=f(V_{DS},V_{GS}); T_J=125˚C

Fig10 Typ. Reverse Characteristics (Q1 & Q2)



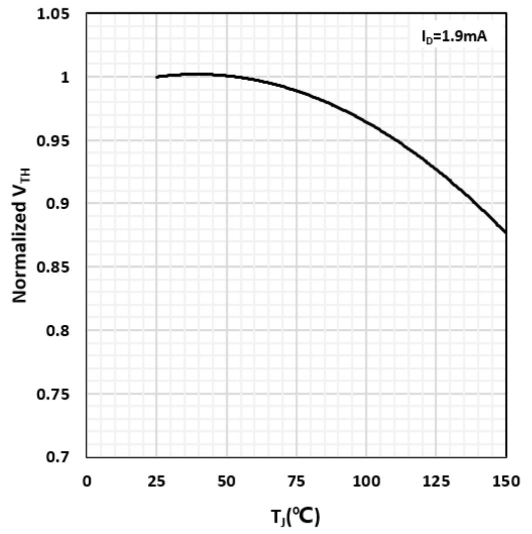
I_D=f(V_{DS},V_{GS}); T_J=125˚C

Fig11 Typ. Capacitances (Q1 & Q2)



C_{xSS}=f(V_{DS}); f=100KHz

Fig12 Threshold Voltage vs Temp. (Q1 & Q2)



V_{TH}=f(T_J); V_{GS}= V_{DS}; I_D=1.9mA

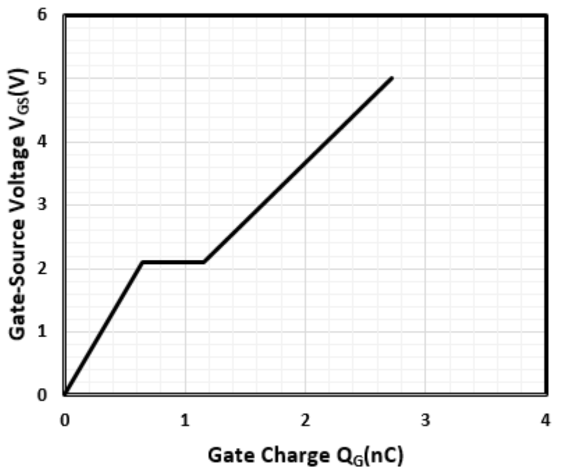
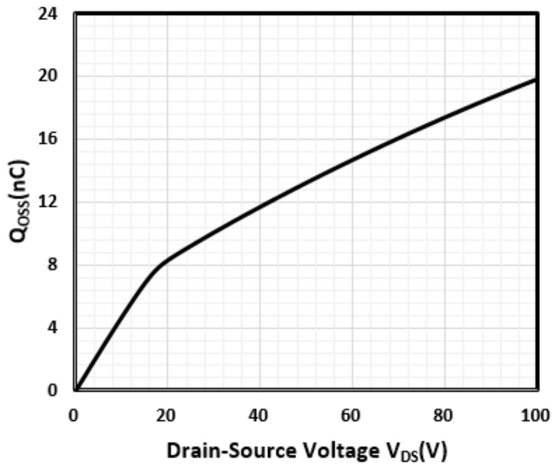
Fig13 Typ. Gate Charge (Q1 & Q2)	Fig14 Output Charge (Q1 & Q2)
	
V_{GS}=f(Q_G); V_{DCLINK}=50V;I_D=7A	Qoss = f(V_{DS})

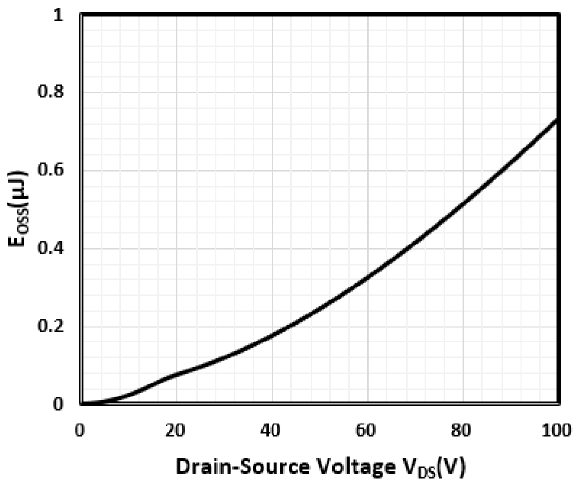
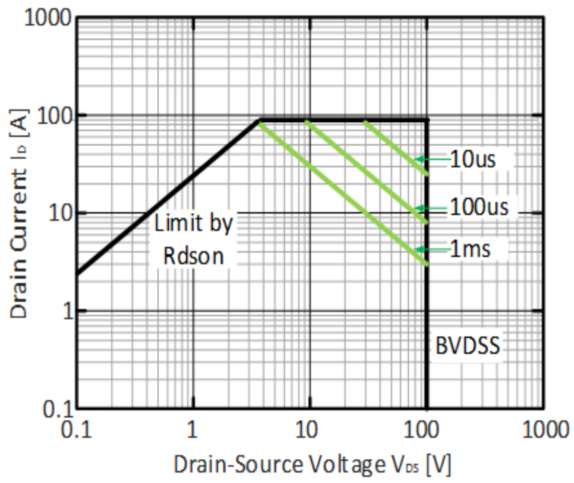
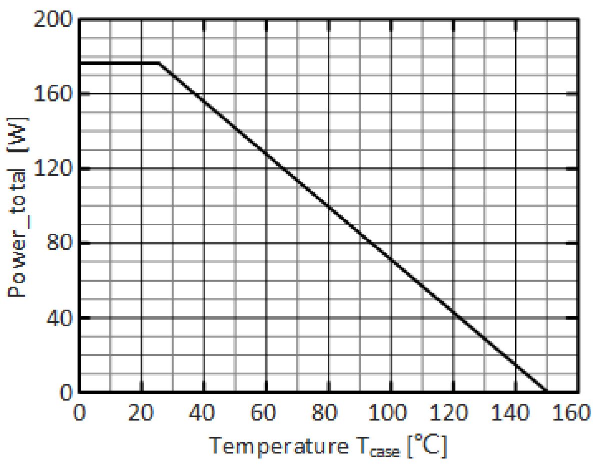
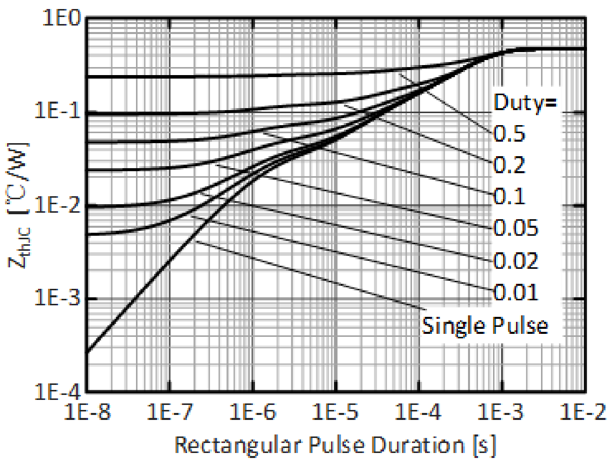
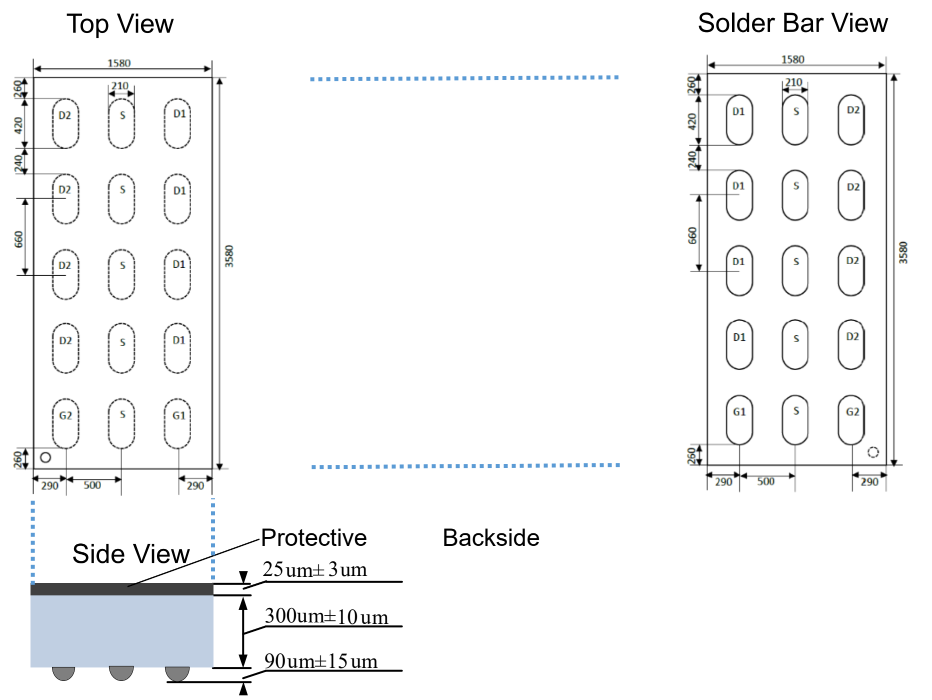
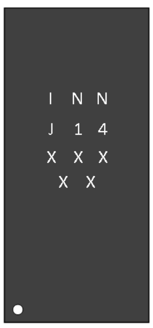
Fig15 Output Capa. Stored Energy (Q1 & Q2)	Fig16 Safe Operating Area (Q1 & Q2)
	
Eoss = f(V_{DS})	I_D=f(V_{DS}) ; T_C=25˚C; parameter: t_p

Fig17 Power Dissipation	Fig18 Max. Transient Thermal Impedance
	
$P_{tot}=f(T_{case})$	Z_{thJC} = f(t_p); parameter: D= t_p / T

Package outlines



Marking Reference



Gate Position

Marking Line 1	Company Code
Marking Line 2	Product Code
Marking Line 3	Lot/ Package Code
Marking Line 4	Lot/ Package Code

Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2020-04-30	1.0 version setup

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