

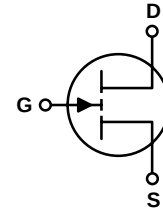
INN030EQ015A

1. General Description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in En-FCQFN with 5 mm x 4 mm package size.

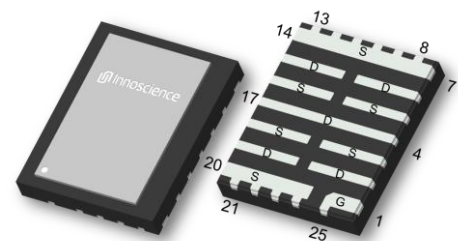
2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Zero reverse recovery charge
- Exposed die for top-side thermal optimization



3. Applications

- High frequency DC-DC converter
- Battery charger
- Battery management system
- Notebook
- Industry



Top View

Bottom View

4. Key Performance Parameters

Table 1 Key Performance Parameters at $T_J = 25\text{ }^{\circ}\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	30	V
$R_{DS(on),max}$ @ $V_{GS} = 5\text{ V}$	1.5	m Ω
$Q_{G,typ}$ @ $V_{DS} = 15\text{ V}$	22.8	nC
$I_{DS,Pulse}$ ($T_J = 25\text{ }^{\circ}\text{C}$)	300	A
Q_{OSS} @ $V_{DS} = 15\text{ V}$	43	nC

5. Pin Information

Table 2 Pin Information

Pin	Pin description	Pin function
1, 25	Gate	Driver Gate
3, 5, 7-14, 16, 18, 20-24	Source	Source
2, 4, 6, 15, 17, 19	Drain	Power Drain

Table 3 Ordering Information

Type/Ordering Code	Package	Product Code
INN030EQ015A	En-FCQFN 5mm x 4mm	C12

Table of Contents

1. General Description.....1

2. Features.....1

3. Applications1

4. Key Performance Parameters1

5. Pin Information.....1

6. Maximum Ratings3

7. Thermal Characteristics4

8. Electric Characteristics5

9. Electric Characteristics Diagrams7

10.Package Outlines12

11.Reel Information.....13

12.Land Pattern.....14

13.Revision History.....15

6. Maximum Ratings

at $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Exceeding the maximum ratings may destroy the device. For further information, contact Innoscence sales office.

Table 4 Maximum Ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	30	V
I_D	Continuous Current ($V_{GS} = 5\text{ V}$, $T_C = 25\text{ }^{\circ}\text{C}$)	183	A
	Continuous Current ($V_{GS} = 5\text{ V}$, $T_C = 100\text{ }^{\circ}\text{C}$)	116	A
	Continuous Current ($V_{GS} = 5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $R_{\theta JA} = 53\text{ }^{\circ}\text{C/W}$)	30	A
	Pulsed Current ($V_{GS} = 5\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, $T_{Pulse} = 300\text{ }\mu\text{s}$)	300	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
P_{tot}	Power Dissipation ($T_C = 25\text{ }^{\circ}\text{C}$)	87	W
	Power Dissipation ($T_A = 25\text{ }^{\circ}\text{C}$)	2.4	W
T_J	Operating Temperature	-40 to 150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature	-40 to 150	$^{\circ}\text{C}$

7. Thermal Characteristics

Table 5 Thermal Characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
R _{θJC}	Thermal Resistance, Junction to Case, Top	0.35	°C/W	
R _{θJC}	Thermal Resistance, Junction to Case, Bottom	1.43	°C/W	
R _{θJA}	Thermal Resistance, Junction to Ambient ¹	53	°C/W	
T _{sold}	Maximum Reflow Soldering Temperature	260	°C	MSL3

Note 1: R_{θJA} is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric Characteristics

at $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 6 Static Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{DSS}	Drain Source Leakage	-	10	100	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 24\text{ V}$
	Drain Source Leakage (125 $^{\circ}\text{C}$)	-	100	1000	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 24\text{ V}$
I_{GSS}	Gate-to-Source Forward Leakage	-	6	60	μA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Forward Leakage (125 $^{\circ}\text{C}$)	-	60	600	μA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Reverse Leakage	-	30	300	μA	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}$	Gate Threshold Voltage	0.9	-	2.1	V	$V_{DS} = V_{GS}$, $I_D = 5\text{ mA}$
$R_{DS(on)}$	Drain-Source On-state Resistance ²	-	1.2	1.5	m Ω	$V_{GS} = 5\text{ V}$, $I_D = 15\text{ A}$
V_{SD}	Source-Drain Forward Voltage	-	1.65	-	V	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$

Note 2: $R_{DS(on)}$ is measured without prior drain bias or switching stress.

Table 7 Dynamic Characteristics ³

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{ISS}	Input Capacitance	-	3.4	-	nF	V _{GS} = 0 V, V _{DS} = 15 V
C _{OSS}	Output Capacitance	-	1.8	-		V _{GS} = 0 V, V _{DS} = 15 V
C _{RSS}	Reverse Transfer Capacitance	-	0.1	-		V _{GS} = 0 V, V _{DS} = 15 V
C _{OSS(ER)}	Energy Related C _{OSS}	-	2.5	-		V _{GS} = 0 V, V _{DS} = 0 V to 15 V
C _{OSS(TR)}	Time Related C _{OSS}	-	2.8	-		V _{GS} = 0 V, V _{DS} = 0 V to 15 V
R _G	Gate resistance	-	1.6	-	Ω	f = 1 MHz
Q _G	Total Gate Charge	-	22.8	-	nC	V _{GS} = 5 V, V _{DS} = 15 V, I _D = 15 A
Q _{GS}	Gate to Source Charge	-	5.5	-		V _{DS} = 15 V, I _D = 15 A
Q _{GD}	Gate to Drain Charge	-	3.2	-		V _{DS} = 15 V, I _D = 15 A
Q _{G(TH)}	Gate Charge at Threshold	-	3.8	-		V _{DS} = 15 V, I _D = 15 A
Q _{OSS}	Output Charge	-	43	-		V _{GS} = 0 V, V _{DS} = 15 V

Note 3: Defined by design. Not subject to production test.

9. Electric Characteristics Diagrams

at $T_J = 25^\circ\text{C}$, unless specified otherwise

Figure 1 Typical Output Characteristics ($T_J = 25^\circ\text{C}$)

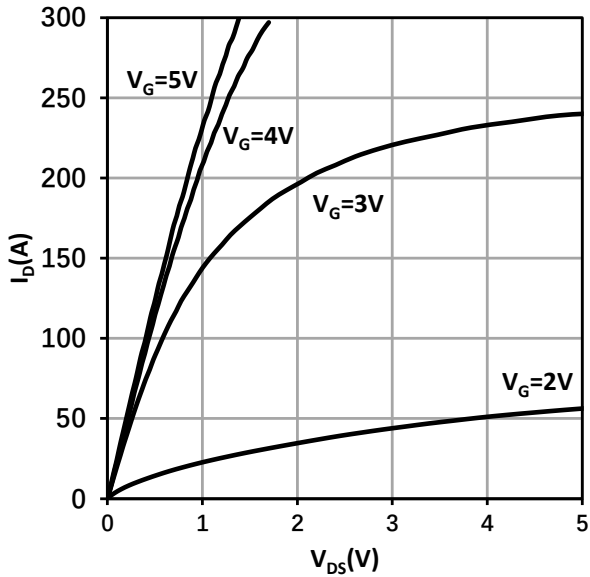


Figure 2 Typical Output Characteristics ($T_J = 125^\circ\text{C}$)

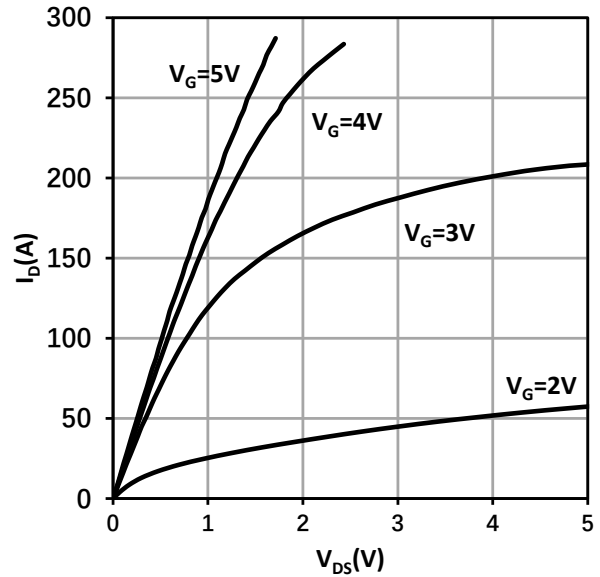


Figure 3 Typical On-state Resistance ($T_J = 25^\circ\text{C}$)

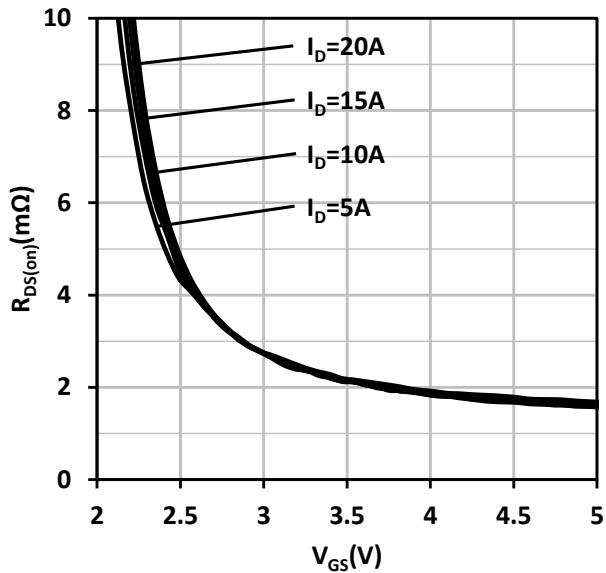


Figure 4 Typical On-state Resistance ($T_J = 125^\circ\text{C}$)

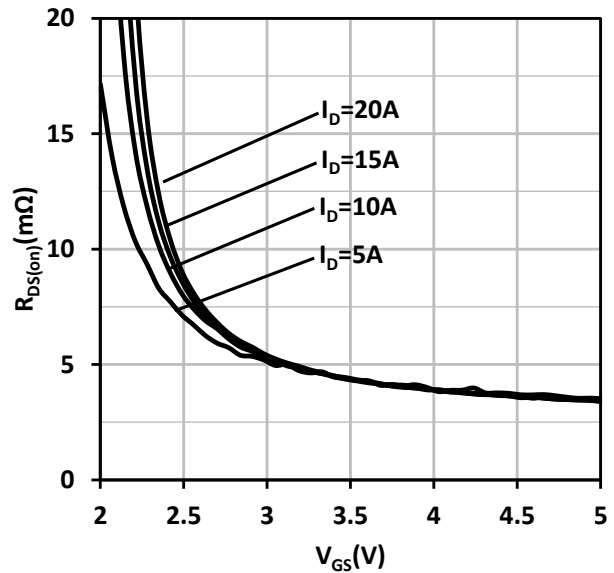


Figure 5 Normalized On-State Resistance vs. Temp.

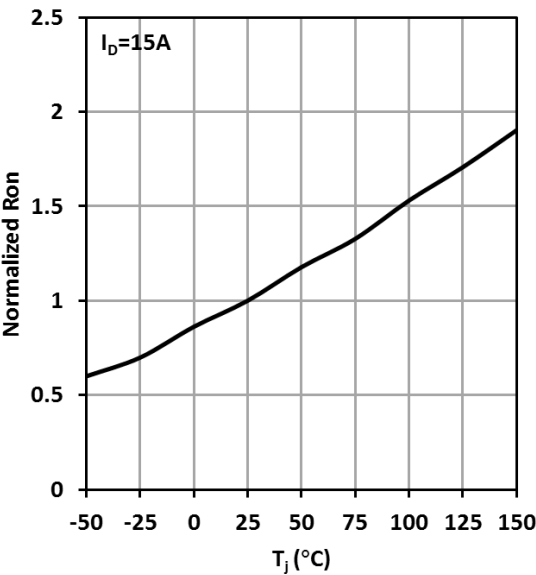


Figure 6 Typical Transfer Characteristics

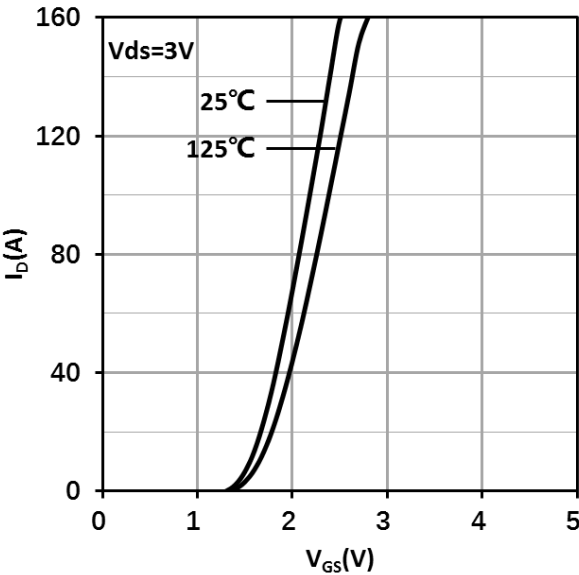


Figure 7 Typical Reverse Characteristics
($V_{GS} \leq 0, T_J = 25^\circ\text{C}$)

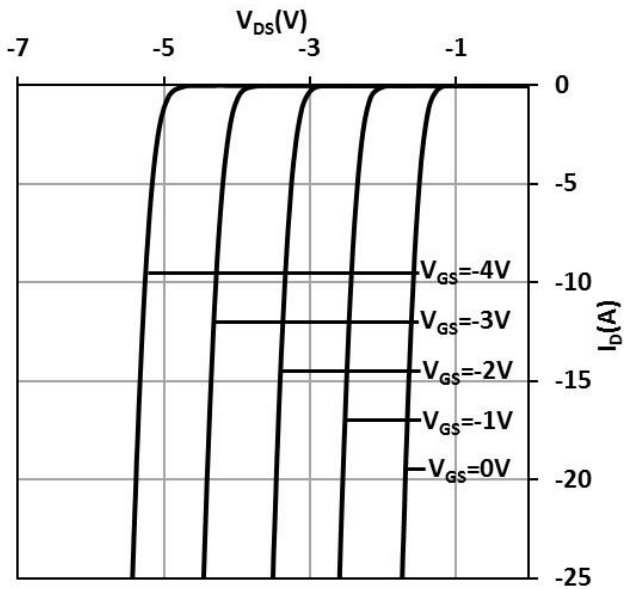


Figure 8 Typical Reverse Characteristics
($V_{GS} \geq 0, T_J = 25^\circ\text{C}$)

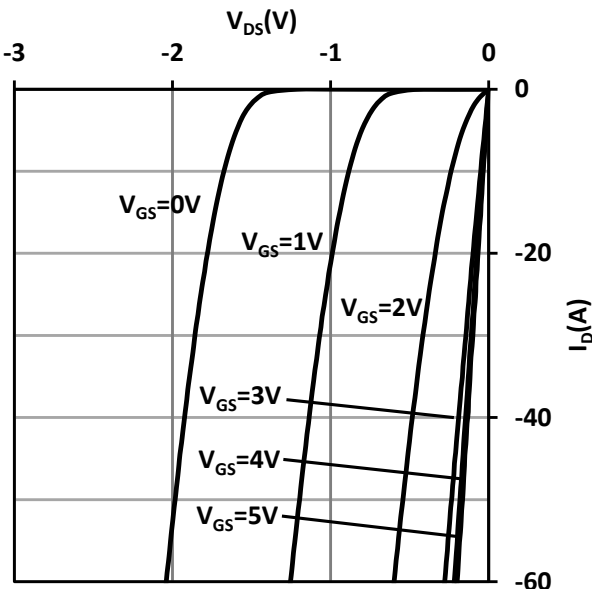


Figure 9 Typical Reverse Characteristics
($V_{GS} \leq 0, T_J = 125^\circ\text{C}$)

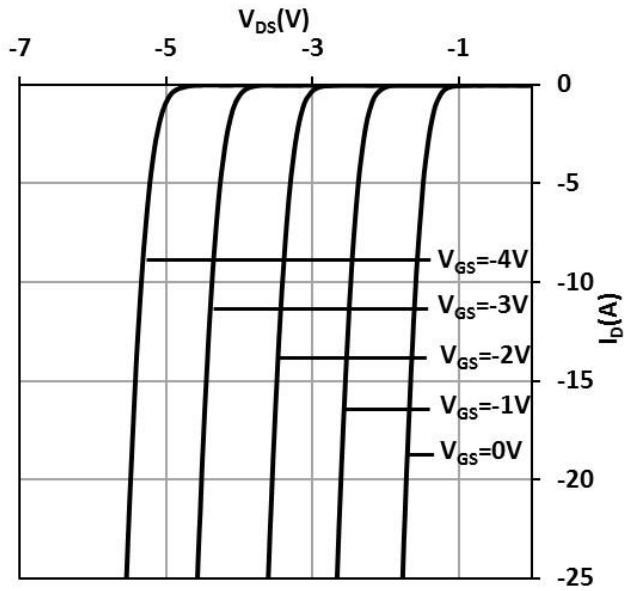


Figure 10 Typical Reverse Characteristics
($V_{GS} \geq 0, T_J = 125^\circ\text{C}$)

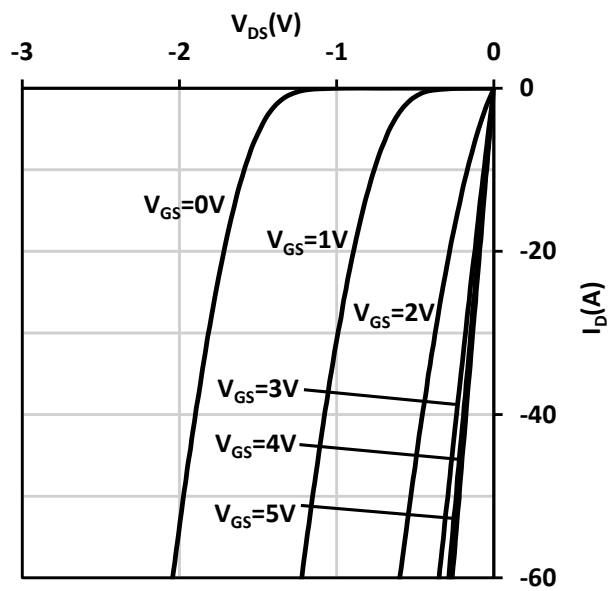


Figure 11 Typical Capacitances Characteristics

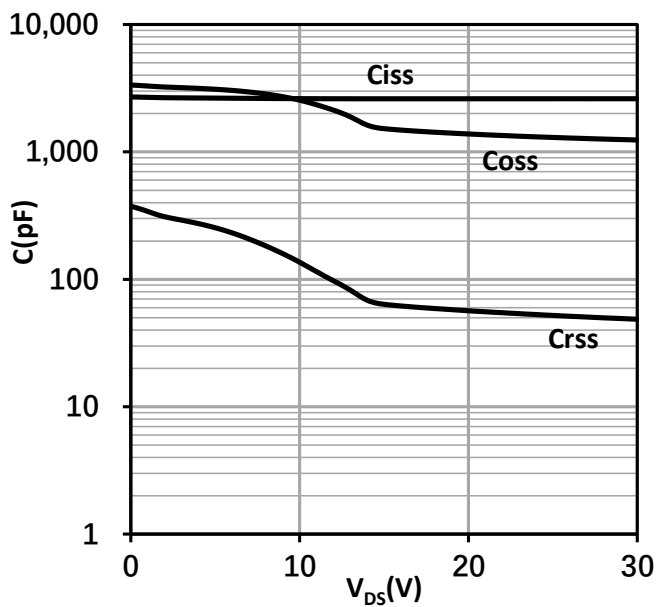


Figure 12 Typical Gate Charge

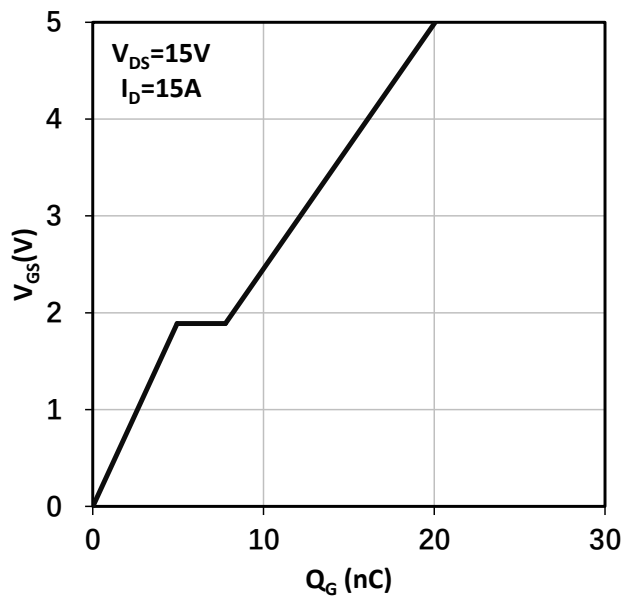


Figure 13 Normalized Threshold Voltage vs. Temp.

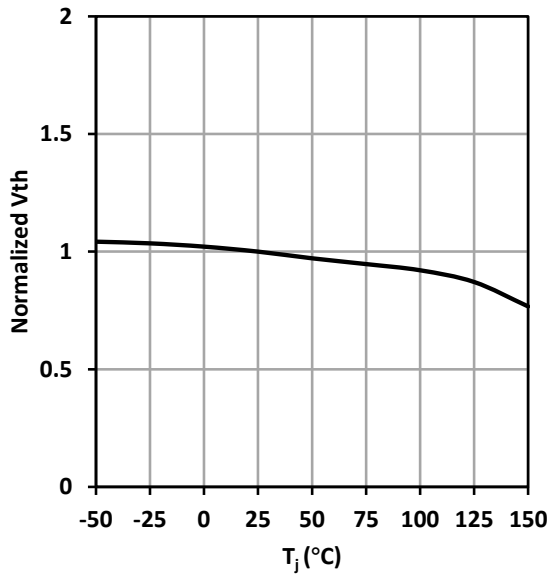


Figure 14 Output Charge

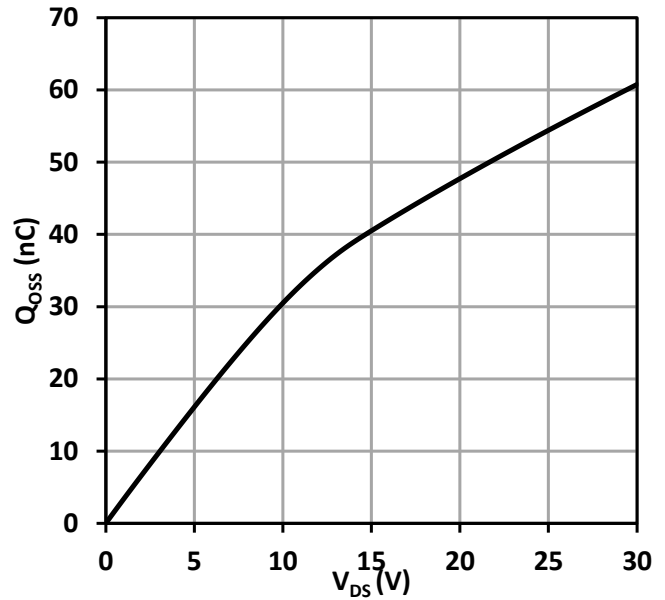


Figure 15 Output Capacitance Stored Energy

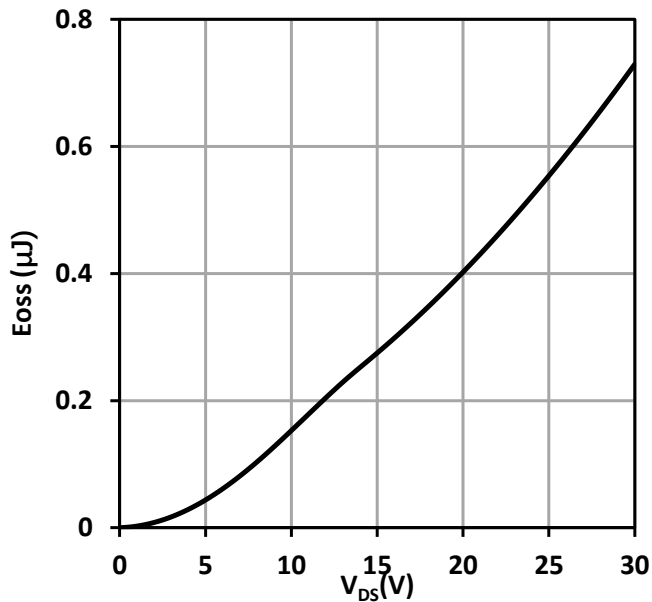


Figure 16 Power Dissipation

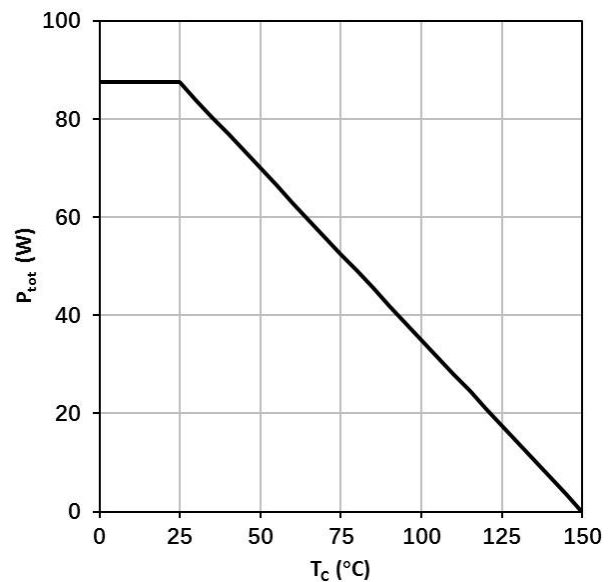


Figure 17 Safe Operating Area

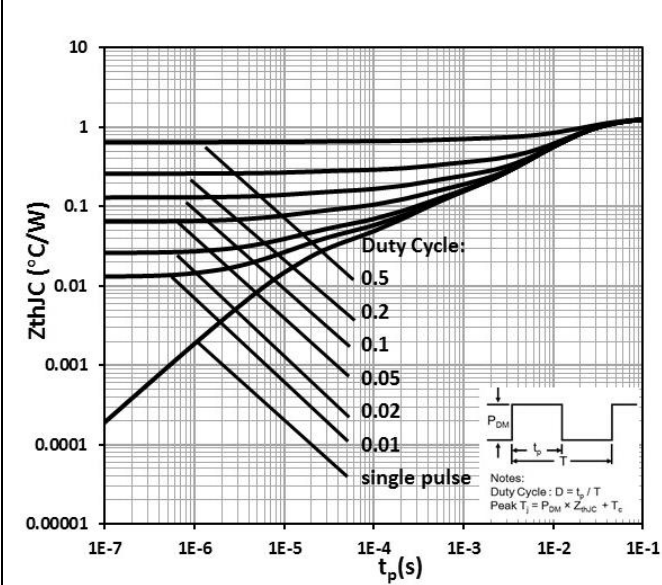
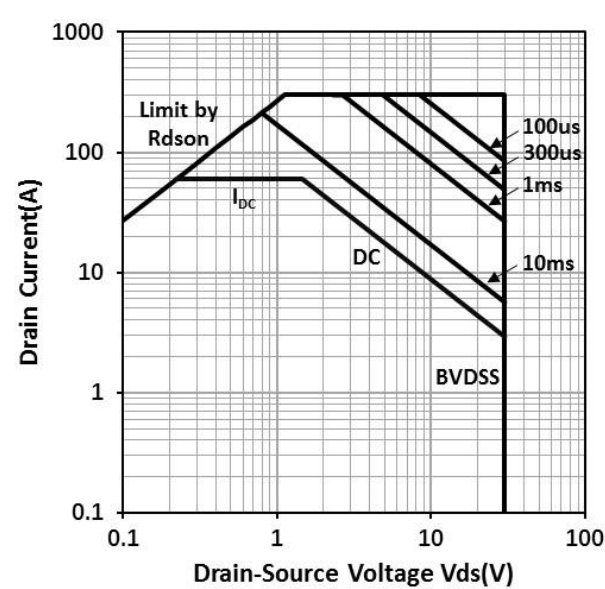
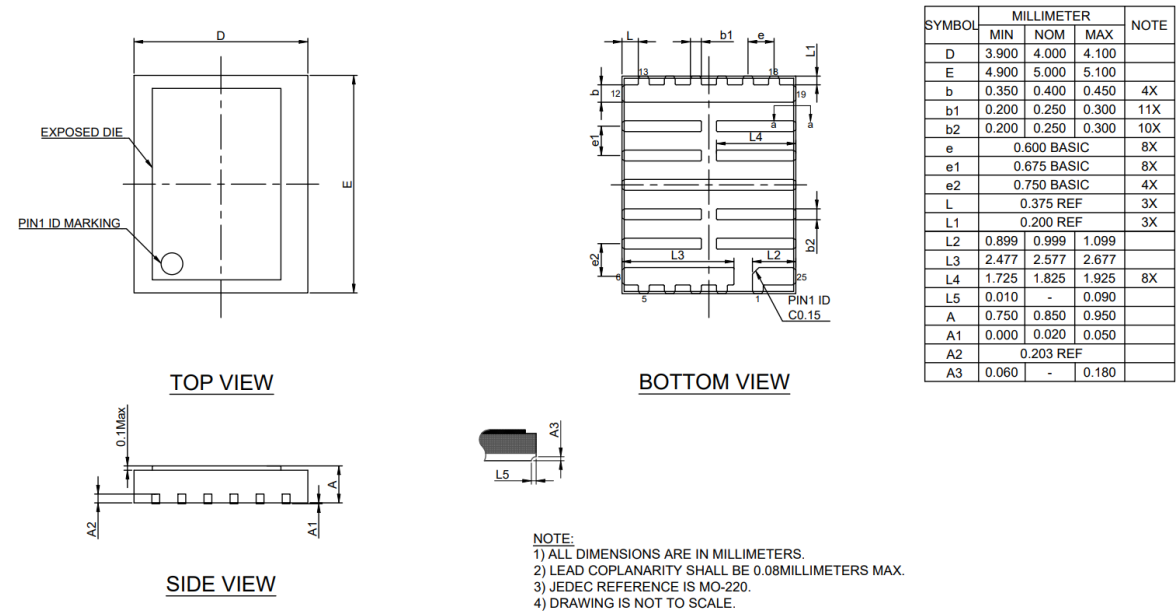


Figure 18 Max. Transient Thermal Impedance

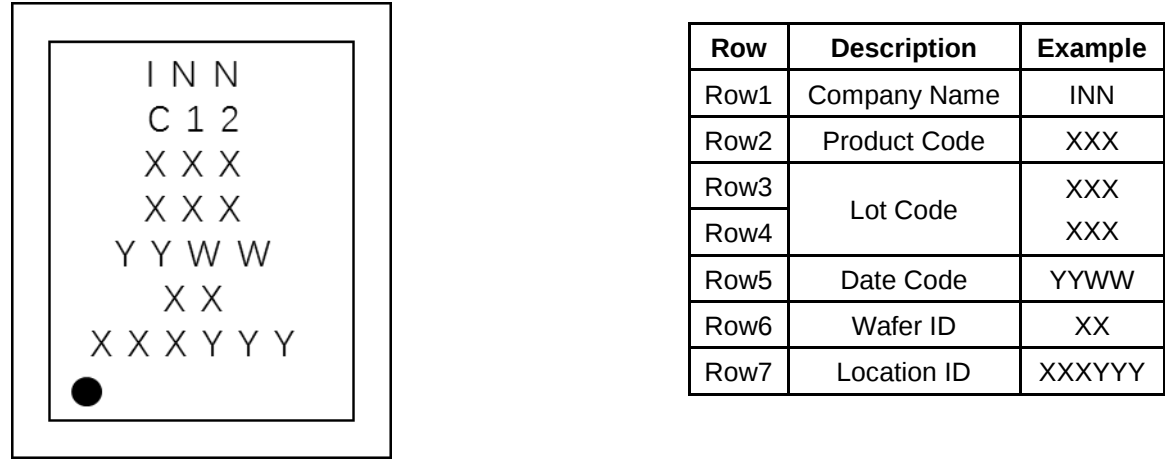


10. Package Outlines

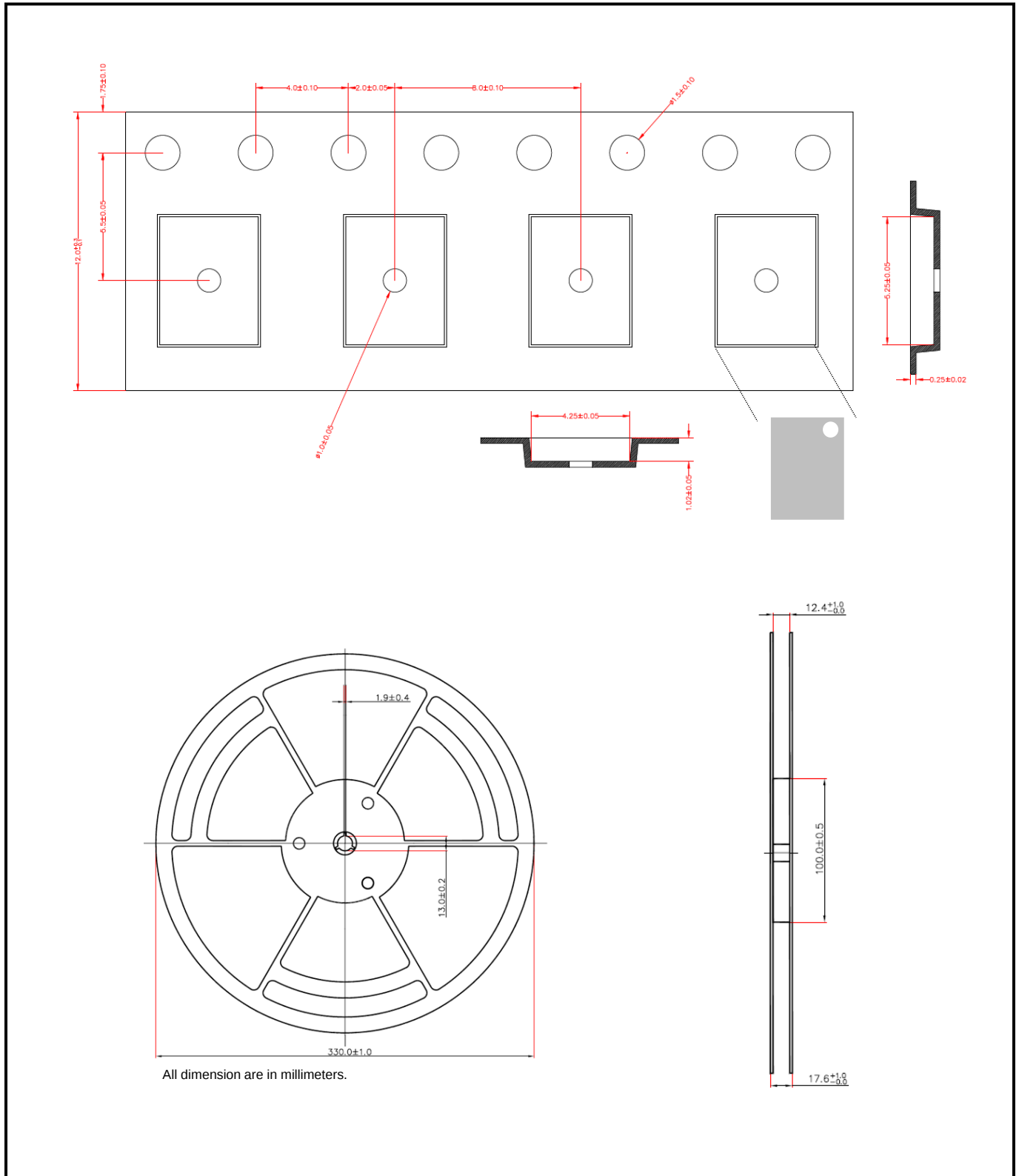
Package Reference



Marking Reference

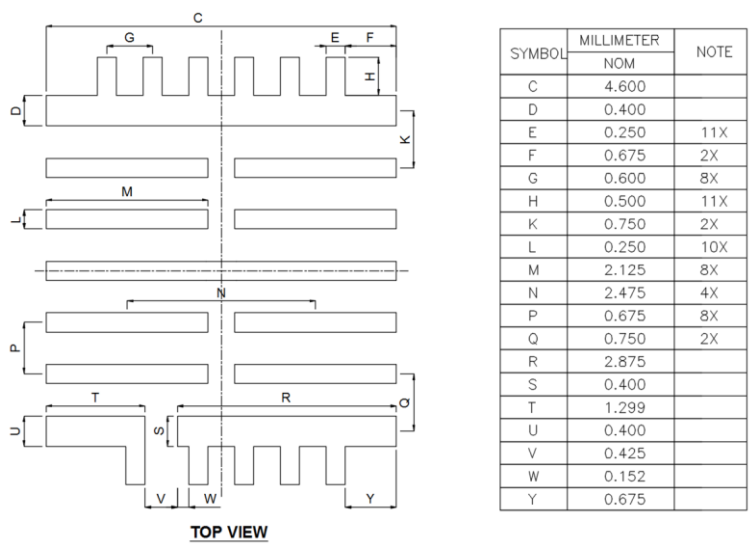


11. Reel Information



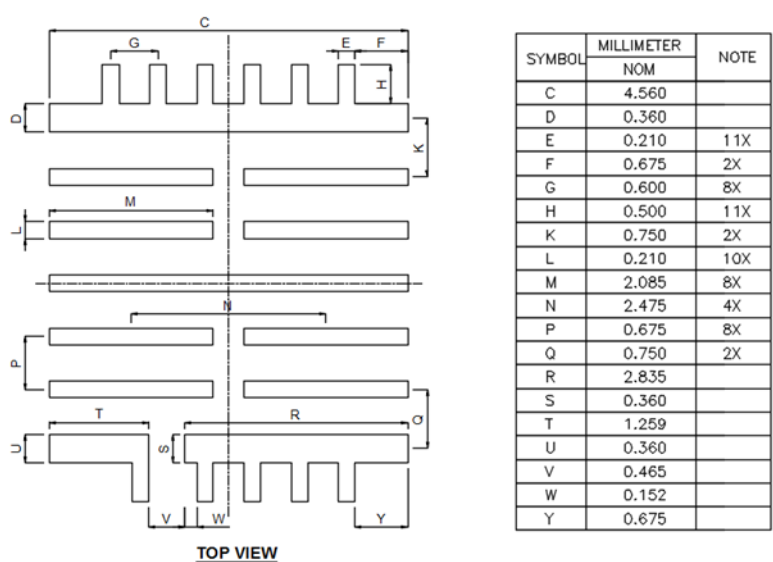
12. Land Pattern

Recommended Land Pattern



- NOTE:
- 1) LAND PATTERN IS SOLDER MASK DEFINED.
 - 2) IT IS RECOMMENDED TO HAVE ON-CU TRACE PCB VIAS.

Recommended Stencil Drawing



13. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2025-05-12	1.0 Version Setup

Important Notice

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