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POWER THE FUTURE

AN011

Application Note

HV InnoGaN High Power Parallel Design Guide

Content

1. Why Paralleling

Due to the continuously increase of power rating, lower on-state resistance RDS(on) is needed for switching transistors. In many applications, one single switching transistors is no longer sufficient for the current capability of the system. Thus parallel connection of multi- devices is needed to reduce the conduction losses and device temperatures, and meanwhile increase the efficiency of power converters. However, engineers have to deal with the issues of imbalanced current and power loss sharing among the paralleled devices due to the sightly asynchronous conduction and turn-on/turn-off processes.

The article focuses on soft switch applications, elaborating on key aspects of parallel design from perspectives such as device drive design and PCB design. For scenarios involving parallel hard switch applications or multi-device parallel applications, please contact INNO FAE for more information.

2. Layout Design of Paralleled InnoGaN

2.1. layout Design Considerations

In order to achieve higher power, multiple GaN devices need to design in parallel in some applications require the use of. This section will discuss the design methods for paralleled multiple GaN devices to achieve performance consistency from the aspects of common-source inductance, power loop, and driving loop designs.

2.1.1. Common-Source Inductance

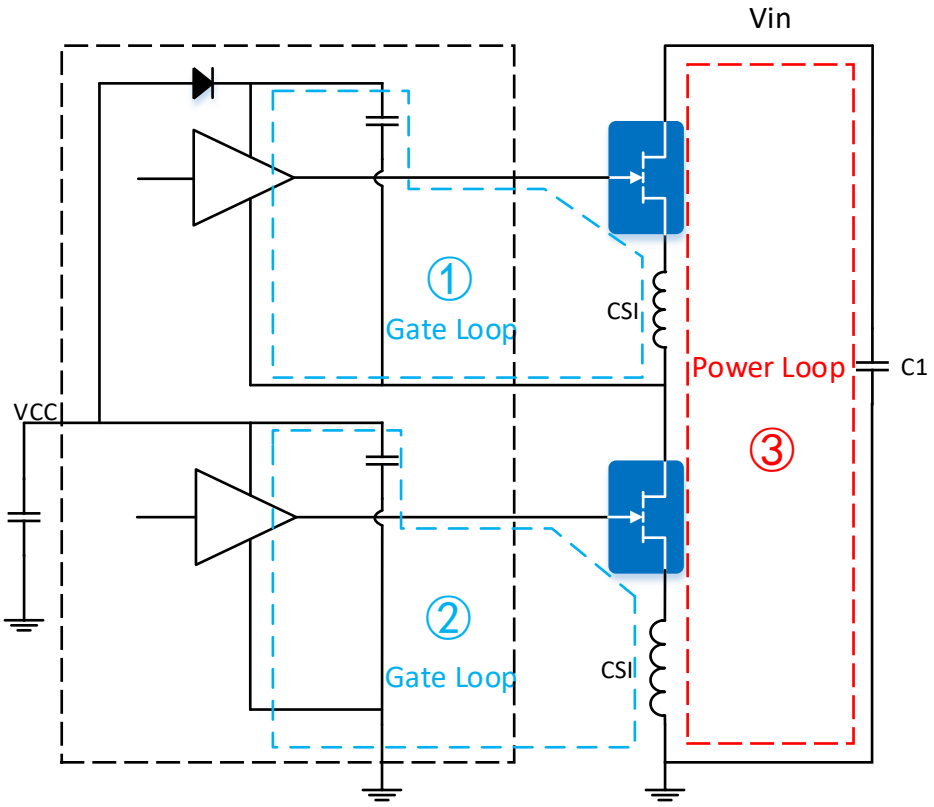

Figure 1 Half-bridge power circuit diagram

Common Source Inductor (CSI) is the common part that gate driving circuit and the power circuit shared at the source terminal of the GaN device as shown in Figure 1.

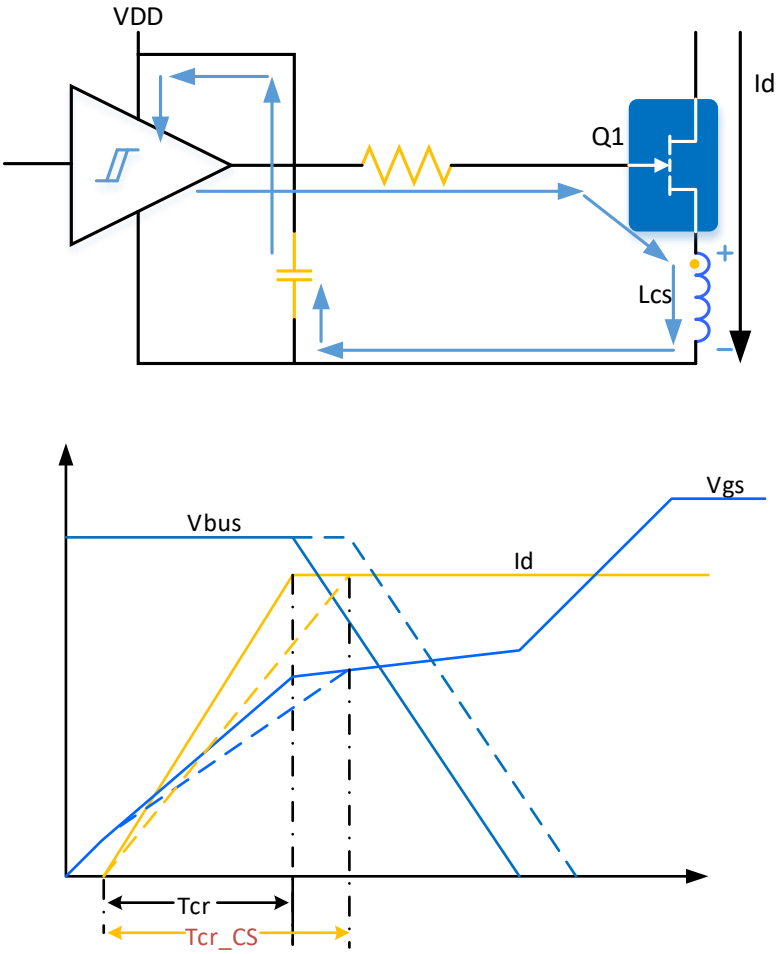

Figure 2 The influence of the common source inductor

During the device turn-on process, the value of di/dt depends on the pull-up/pull-down capability of the driving circuit. With the common source inductor, the drain current slew rate di/dt will generate a negative voltage across the common source inductor during the turn-on process. Therefore the current that charges the gate capacitance is reduced, leads to extended transition time Tcr, increased turn-on losses, and lower efficiency. Attention should be paid to the common source inductor in paralleled InnoGaN design.

2.1.2. Power Loop

Reducing parasitic inductance is crucial for the layout design of high-frequency power devices. The recommended PCB layout design method is as shown in Figure 3.

1. Place MLCC close to the high side InnoGaN for high-frequency signal decoupling.
2. Use the top layer as the power loop forward path while the second inner layer as return path to form the smallest loop size. By this design approach the magnetic fields self-cancellationcould reduce the parasitic inductance in the power loop and benifit to reduce the voltage spikes and improve power efficiency.
3. Parallel devices should be symmetrically placed, withthe same number of vias for each device to ensure the same current capability.
4. Positioning busbars between parallel devices can significantly enhance current sharing and achieve thermal balance.

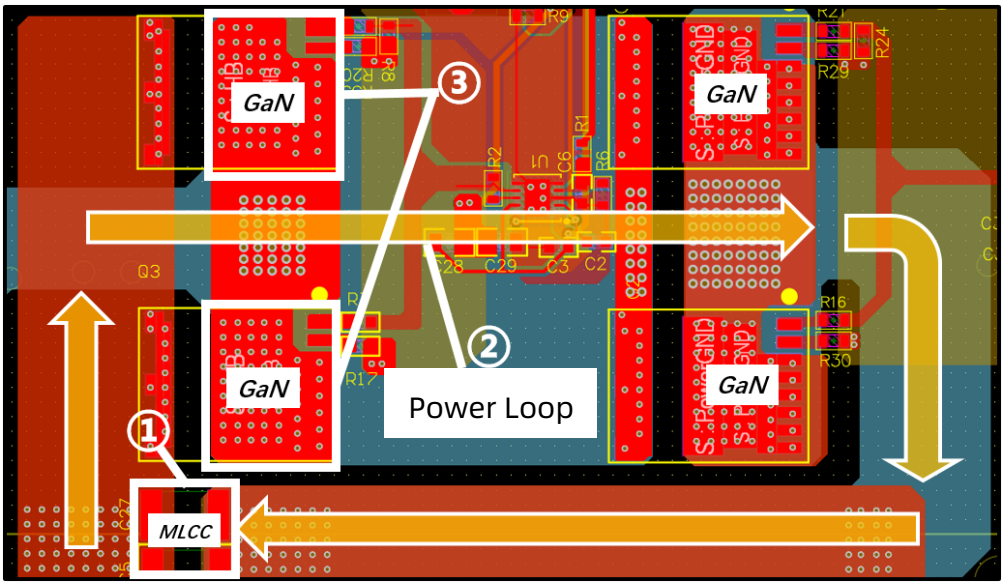

Figure 3 Recommended PCB layout of power loop

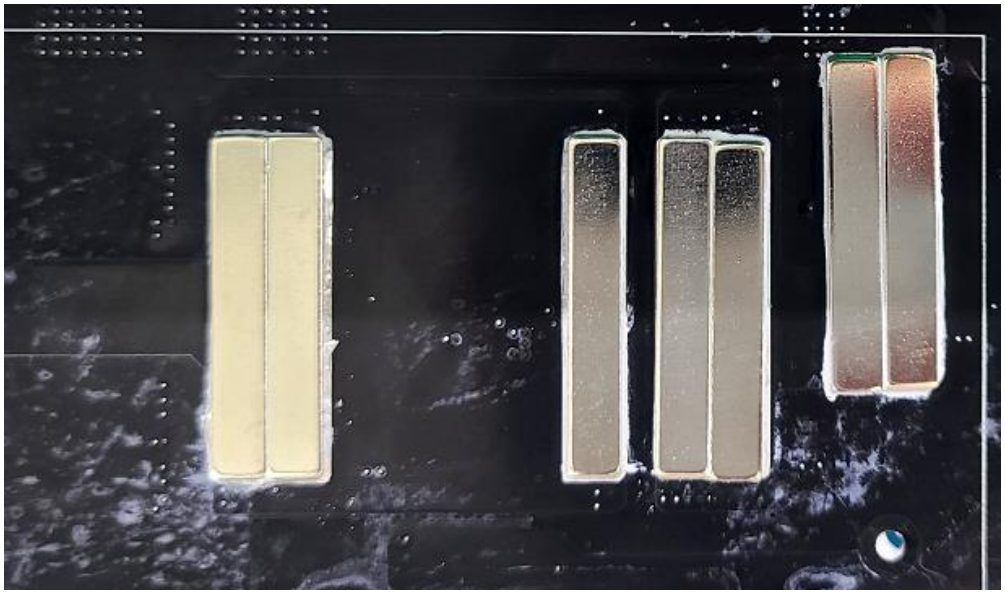

Figure 4 Positioning busbar reserves

2.1.3. Driving Loop

Based on the driving design guide provided in "AN001 High-Voltage InnoGaN Driver Design Guide", it is recommended to share the components in driving circuits as much as possible for parallel driving design. Q1A and Q1B share the driving resistors R4 and R10 to ensure the consistency of driving performance. R5 and R7 should be placed near the Gate terminal which could effectively suppresses the ringing caused by the long driving loop. Additionally, the Kelvin design separates the driving loop and the power loop and reduces the effects of CSI (Common Source Inductance) effectively.

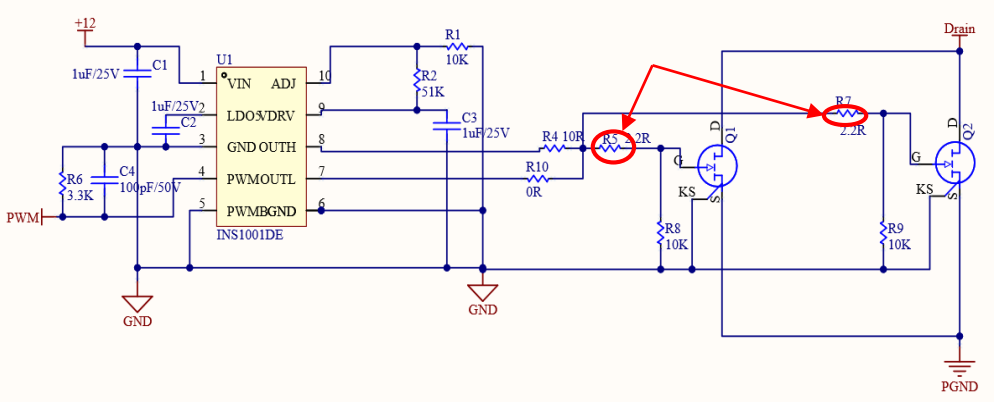

Figure 5 Driving design for paralleled InnoGaN

For PCB design of driving loop in parallel, the recommended PCB layout design method is as follows:

1. Ensure consistent length for both the turn on and turn off paths. Ensure consistency of driving signals.
2. Place driving resistor close to GaN.
3. Through the Kelvin design separates the driving loop and the power loop and reduces the effects of CSI (Common Source Inductance) effectively.
4. The reference ground of the second-layer driving circuit is expanded to effectively reduce parasitic inductance in the circuit. Meanwhile, it can shield the driving from radiated interference caused by the switching node SW.

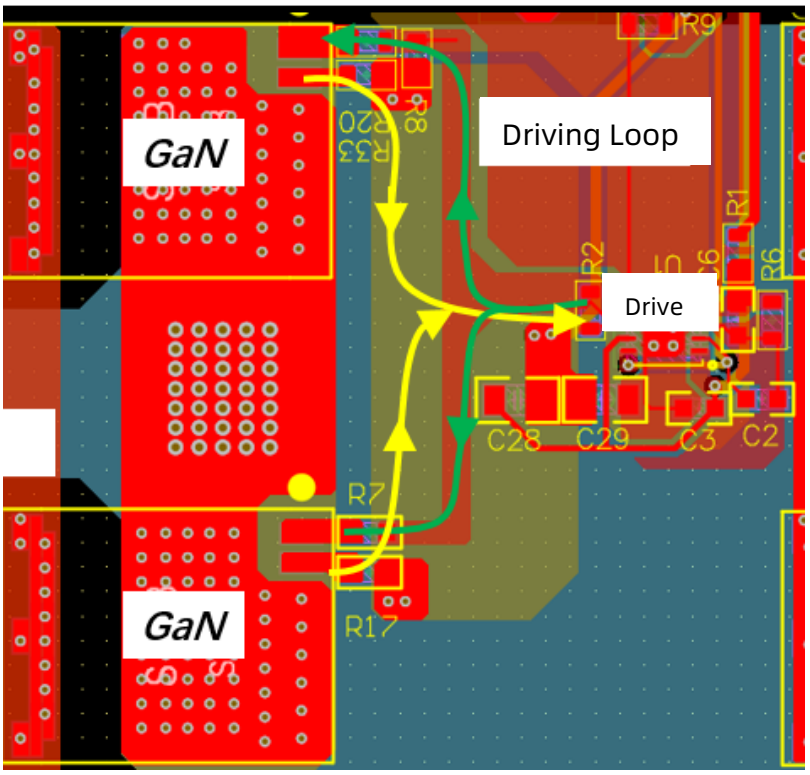

Figure 6 Recommended PCB layout of driving loop

2.2. Paralleled InnoGaN Design

2.2.1. Parallel InnoGaN Design in Single-FET Topology

Applying paralleled multiple devices in single FET topologies introduces complexity to the system layout when taken various current paths of each devices into consideration;

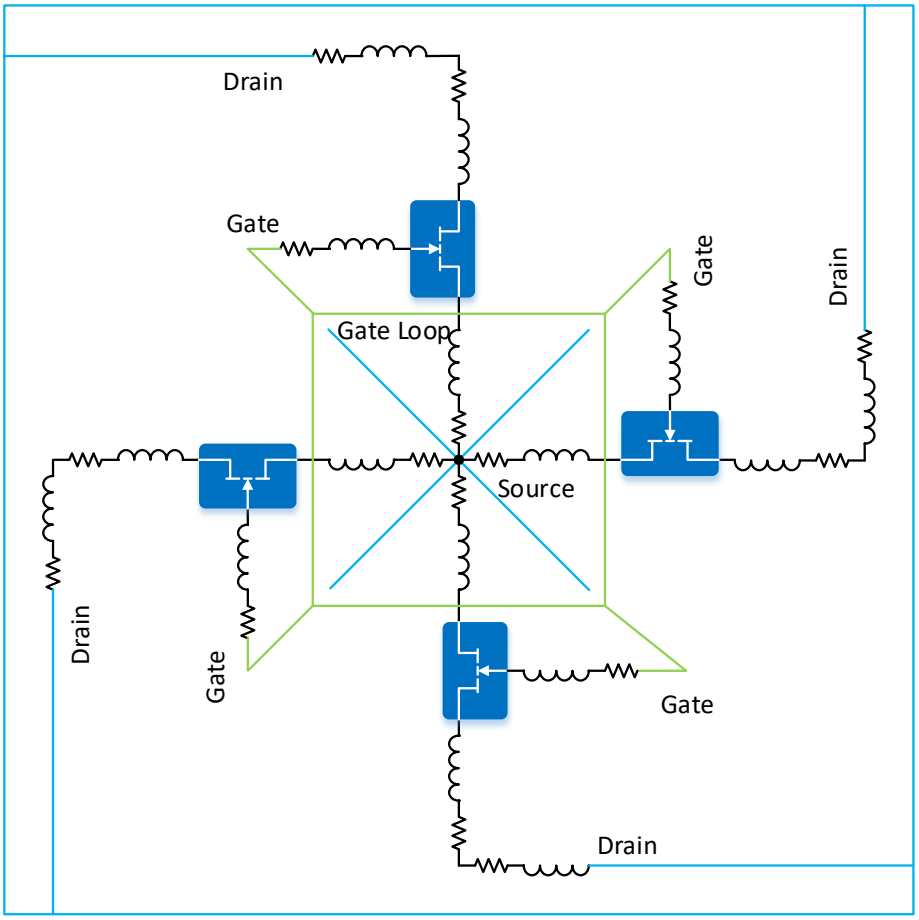

Figure 7 Diagram of Symmetry layout (applicable to high-speed switching applications)

To meet the requirement of symmetry layout of GaN devices, a design example is shown in Figure 7 with the symmetry of the power loop, the common source inductance (CSI), and gate driving loops. As the number of paralleled GaN devices increases, complete symmetry in the layout becomes more difficult to achieve. Therefore, priority should be given as follows:

1. Symmetry in the Common-Source Inductance;
2. Power Loop;
3. Gate Loop;

2.2.2. Paralleled InnoGaN Design in Half-Bridge Topology

Although the layout method for single-FET topologies is also appliable, it may not be the most optimal layout solution for half-bridge topologies. The recommended solution is the mirror symmetry methodas shown in Figure 8.

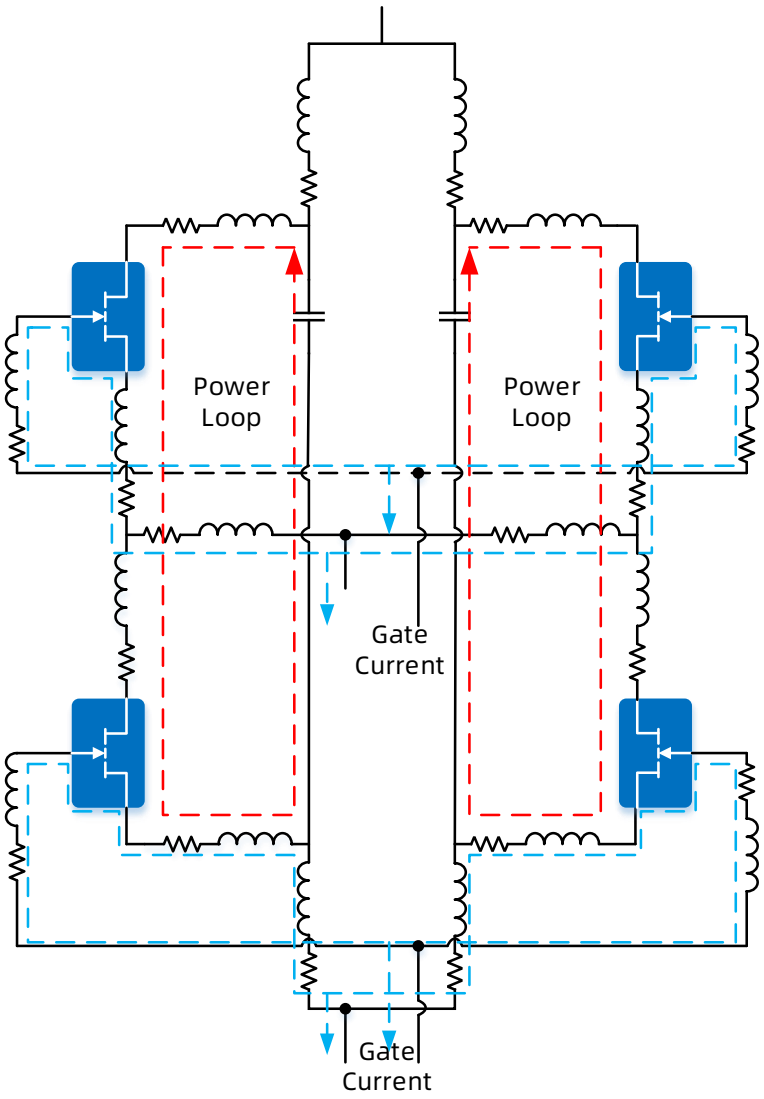

Figure 8 Half-bridge symmetrical layout diagram

The symmetrical scheme realizes a reliable parallel connection for multiple GaN devices in half-bridge topologies. It features independent power loops, which not only reduce the total loop parasitic parameters but also ensure the consistency of each parasitic parameters, providing the most balanced performance of each device.

3. Design Examples of Paralleled InnoGaN

3.1. Paralleled InnoGaN Design in 3kW PSU

Based on the design considerations in the previous sections, the actual performance is validated in a low 3kW TCM mode PSU circuit. The system employs 2 HV InnoGaNINN650TA030AH in parallel in front-end PFC with the system frequency of 65kHz

Test conditions: input voltage 230V, PFC output 390V & 3kW, burn-in 1 hour. The actual parallel connection performs well and the temperature of the paralleled device casing is balanced as shown in Figure 9:

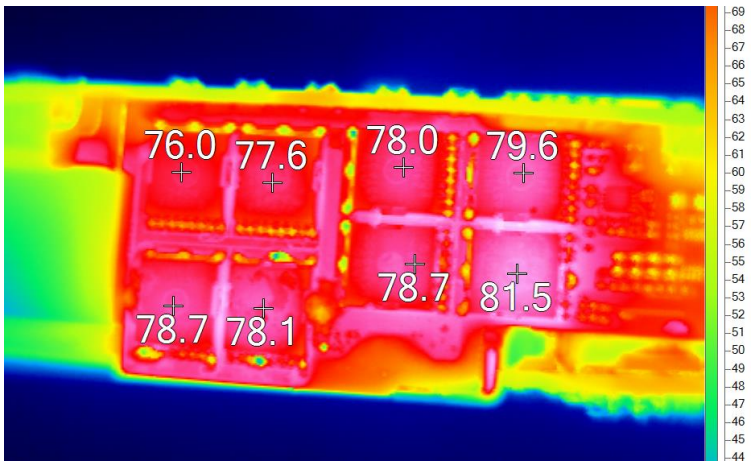

Figure 9 3kW Measured casing temperature

3.1.1. Driving Design

According to the design considerations mentioned above, the paralleled GaN FETs share the driving resistors RP23 to ensure consistency of gate driving parameters. Additional resistors RP43 and RP44 are employed near the Gate terminal of both GaN FETs to suppress ringing caused by the parasitic parameters in driving loop.

1. Selection of turn-on gate driving resistance: The value of turn-on gate driving resistance depends on parameters such as the Vcc voltage of the controller, gate leakage current, EMI, etc. In this case RP12 is selected as 12Ω.
2. The pull-down resistor RP22 is usually selected with between 10-20K empirically.

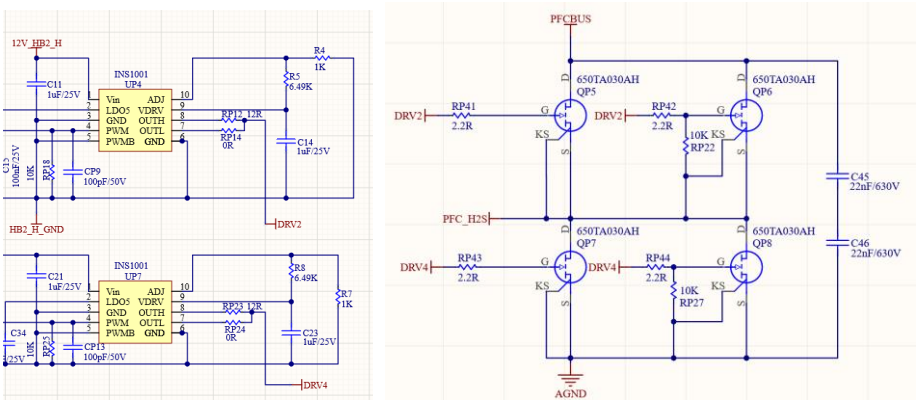

Figure 10 Design Example of Driving Parameters

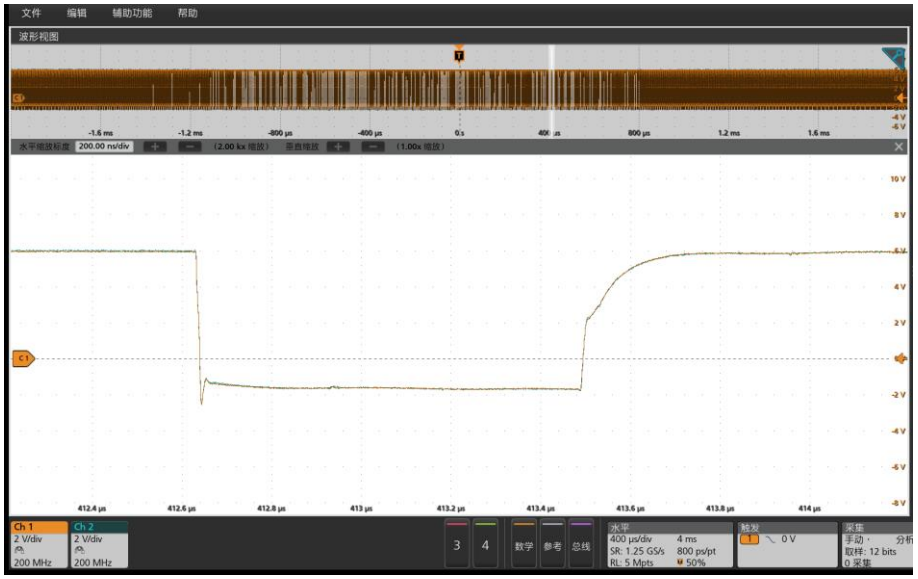

Figure 11 Measured waveforms

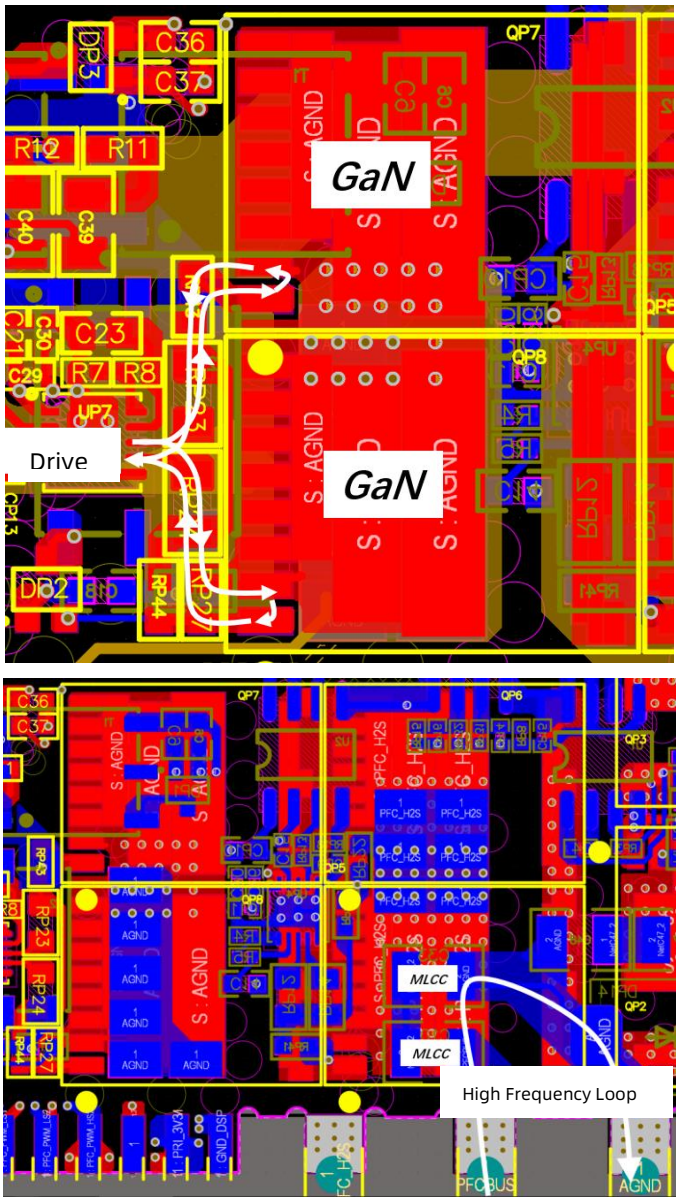

Figure 12 PCB Layout

Revision History

Date	Version	Description	Author
2024/08/09	1.0	English translation	AE team

Note:

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.

Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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