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POWER THE FUTURE

AN010

Application Note

HV InnoGaN Low Power Parallel Design Guide

Content

1. Why Paralleling

Due to the continuously increase of power rating, lower on-state resistance RDS(on) is needed for switching transistors. In many applications, one single switching transistors is no longer sufficient for the current capability of the system. Thus parallel connection of multi- devices is needed to reduce the conduction losses and device temperatures, and meanwhile increase the efficiency of power converters. However, engineers have to deal with the issues of imbalanced current and power loss sharing among the paralleled devices due to the sightly asynchronous conduction and turn-on/turn-off processes.

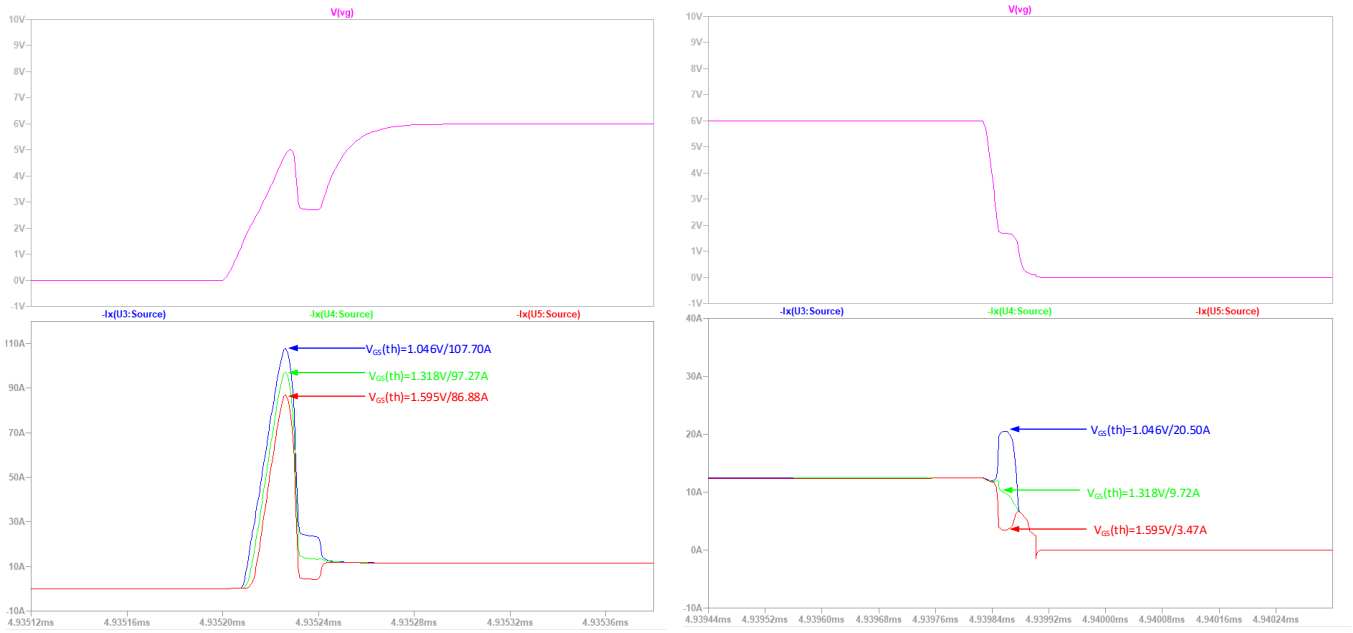
2. Characteristics of Paralleled HV InnoGaN

In this appication note, the reason of why HV InnoGaN is suitable for parallelling in low power applications will be demonstrated from the aspects of VGS(th), RDS(on), and Gm.

2.1. Threshold Voltage VGS(th)

For power devices, VGS(th) represents the turn-on threshold voltage . The device stops conducting current when the gate driving voltage is below the threshold voltage. For GaN power devices, the threshold voltage is the voltage at which the 2-dimensional electron gas (2DEG) beneath the gate is completely depleted. When multiple GaN devices are paralleled, the relationship between VGS(th) and TJ (junction temperature) needs to be considered.

A boost converter with three paralleled InnoGaN is taken as an example for simulation. to analize the current sharing performance between GaN devices with different VGS(th)during turn-on and turn-off processes.



(a) (b)

Figure 1 Current sharing between InnoGaN with different Vgs(th) (a) Turn-on process, (b) Turn-off process

It is observed from the simulation results that higher current flows through the device with smaller threshold voltage (VGS(th)) during both turn-on and

turn-offprocesses, resulting in higher switching losses.

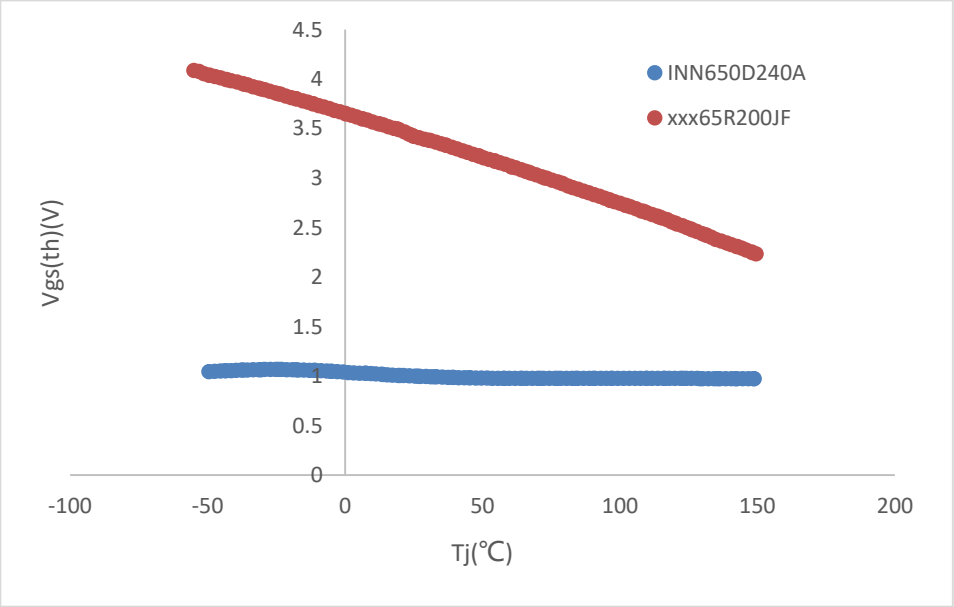


Figure 2 The relationship between VGS(th) and TJ

Based on the relationship between VGS(th) and TJ as mentioned above, it could be concluded that Tj has high significant influence on VGS(th) for Si power devices. Devices with lower threshold voltages suffer from increased turn-off losses, leading to higher overall losses. Then with increased TJ, decreased VGS(th) resulting in even higher current flow and losses, which exacerbats the unbalanced current sharing and is unsuitable for parallelling. However, the VGS(th) of HV InnoGaN is relatively stable with to the variation of TJ, which benifits parallelling application.

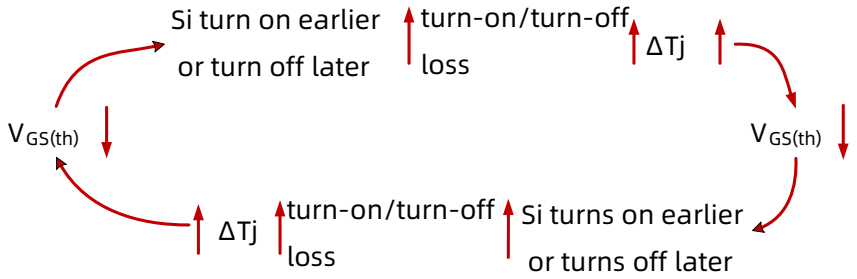


Figure 3 The relationship between VGS(th) and TJ for Si devices when paralleled

2.2. On-State Resistance $R_{DS(on)}$

The on-state resistance, RDS(on), refers to the sum of all resistances within the device. When paralleled GaN devices are in on-state c, smaller

RDS(on) results in a higher current, while larger RDS(on) leads to a lower current on the contrary.

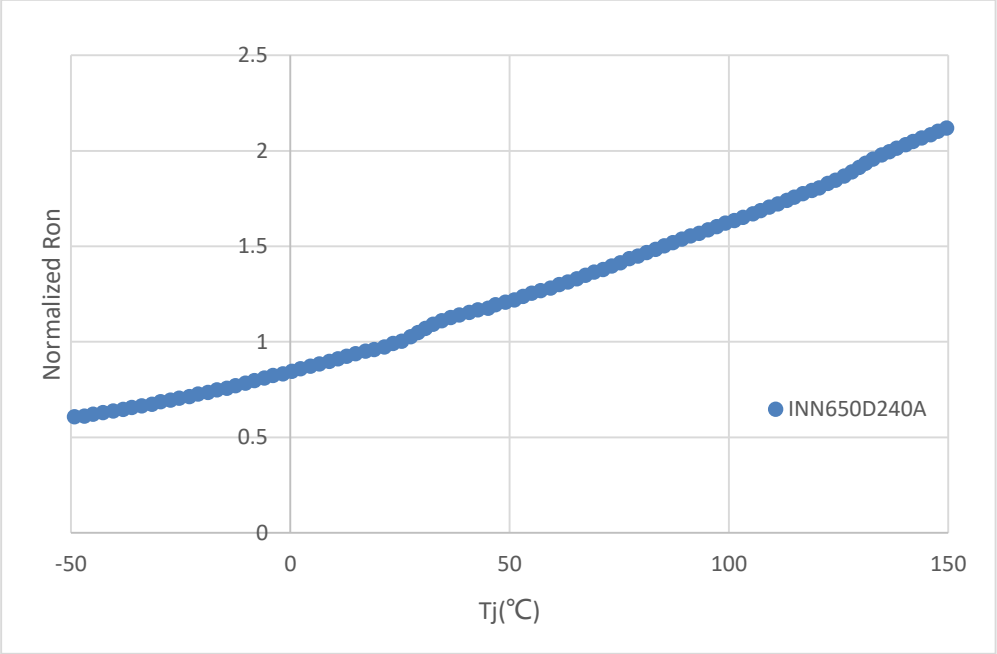


Figure 4 The relationship between RDS（on）and TJ

The relationship between RDS(on) and TJ shown as above in Figure 4. The temperature coefficient between RDS(on) and TJ is positive, which means that RDS(on) increases with TJ, Based on the formula P=(U^2)/(RDS(on)), it can be deduced that the conduction loss increases with a lower TJ. Then RDS(on) of the device increases and pwer loss decreases when TJ rises, forming a negative feedback and eventually balanced current sharing.

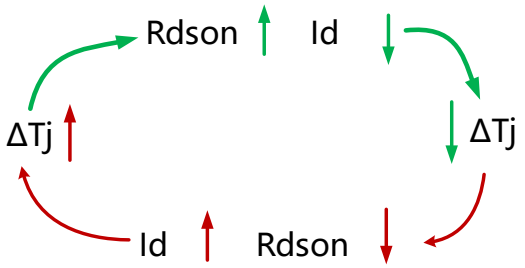


Figure 5 The relationship between GaN RDS(on) and TJ

2.3. Transconductance Gm

The transconductance Gm represents the control of Vgs voltage to the channel current, which could be expressed as follows:

$$Gm = \Delta Id / \Delta Vgs.$$

With the same ΔVgs, a larger Gm corresponds to a larger current flowing through the channel.

Simulation results are obtained to show the current distribution in a Boost converter with three GaN devices in parallel and with different Gm. The simulation results are shown as Figure 6.

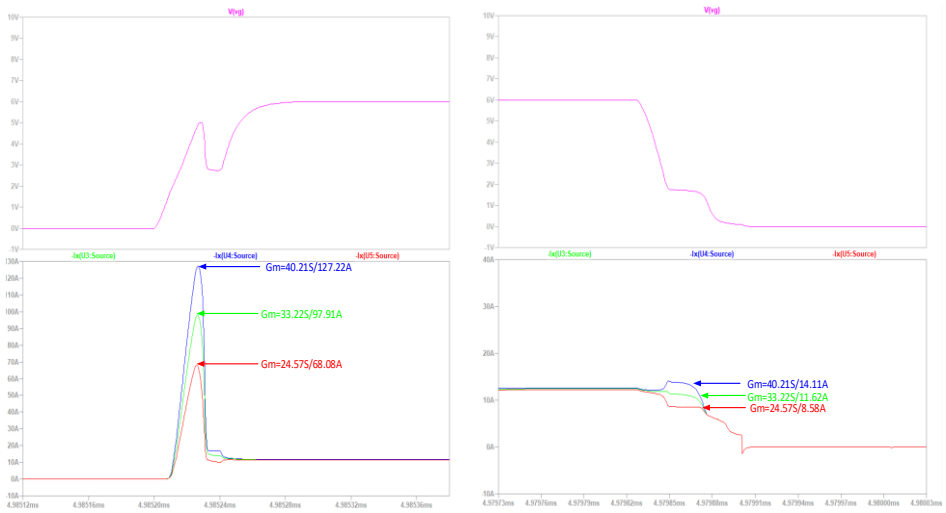


Figure 6 Current distribution with different Gm during switching processes

The simulation results indicates that larger Gm leads to higher current passing through the devices during turn-on and turn-off processes. This is because a larger Gm results in a higher current capability during both turn-on and turn-off transents, and thus the switching losses are higher.

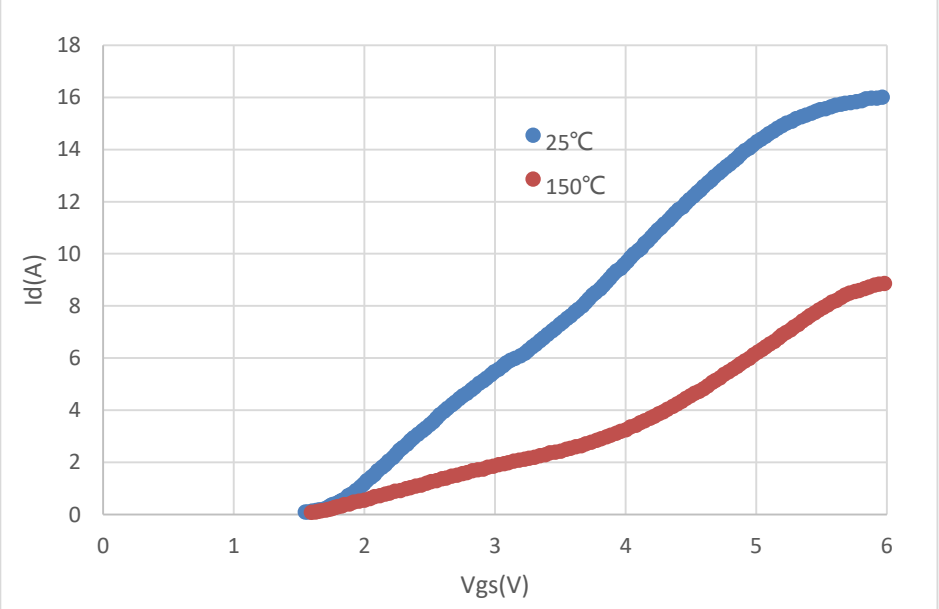


Figure 7 The transfer characteristics of INN650D240A at different temperatures.

The transfer curves for HV InnoGaN INN650D240A are shown in Figure 7, where Gm decreases slowly as TJ gradually increases. together, The devices with higher Gm conduct a greater portion of the turn-on and turn-off current when paralleled, leading to the increase of switching losses and overall device losses. However, Gm decreases with increased TJ, resulting in a reduction of the currents sharing and decreased losses. This will eventually form a balanced status between paralleled devices.

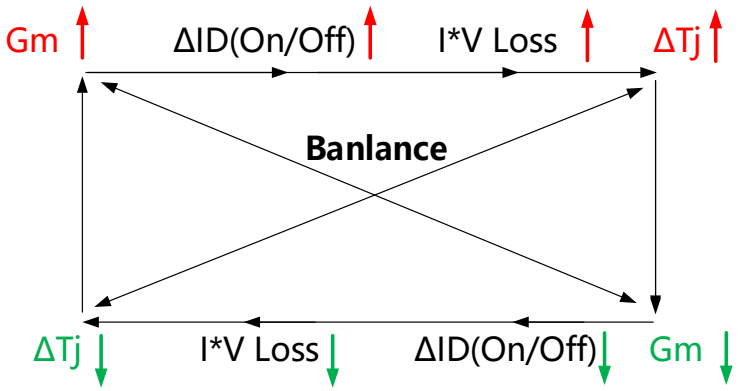


Figure 8 The relationship between Gm and TJ of paralleled InnoGaN

2.4. Summary

After analyzing the feasibility of parallel connection based on VGS(th), RDS(on), and Gm of InnoGaN, it is concluded that InnoGaN is suitable for parallelling applications. The impact of these three key parameters on parallel connection are summarized as in Table 1.

Table 1 Impact of three parameters to parallel connection

Parameters	Symbol	Impact when reduced	Significance
Gate Threshold Voltage	VGS(th)	Turn-on loss increase Turn-off loss increase	The greater the difference in VGS(th), the higher the difference in turn-on and turn-off currents, the higher impact on parallel connection
Transconductance	Gm	Turn-on loss decrease Turn-off loss decrease	The higher the difference in Gm, the higher the difference in turn-on and turn-off currents, the more severe the impact on parallel connection
On-state Resistance	RDS(on)	conduction loss decrease	In GaN HEMT parallel connection, Ron and Tj are dynamically balanced, with relatively minor impact

3. Layout Design of Paralleled InnoGaN

3.1. PCB layout Design Considerations

In order to achieve higher power, multiple GaN devices need to design in parallel in some applications require the use of. This section will discuss the design methods for paralleled multiple GaN devices to achieve performance consistency from the aspects of common-source inductance, power loop, and driving loop designs.

3.1.1. Common-Source Inductance

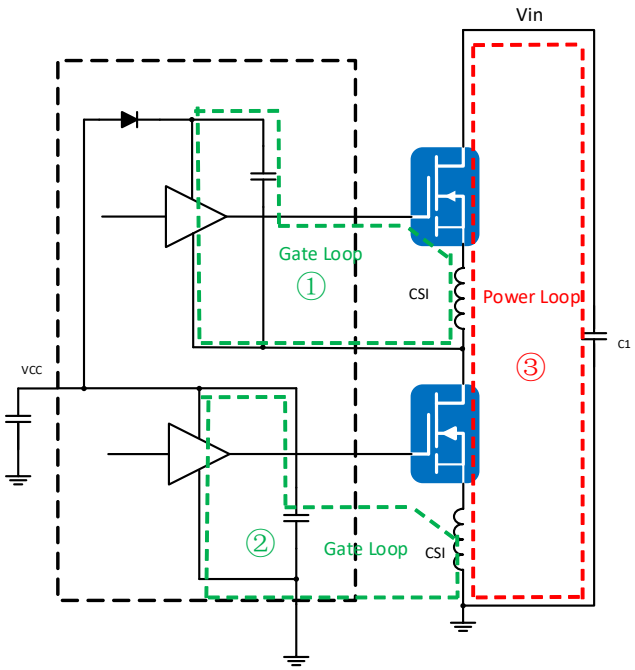


Figure 9 Half-bridge power circuit diagram

Common Source Inductor (CSI) is the common part that gate driving circuit and the power circuit shared at the source terminal of the GaN device as shown in Figure 9.

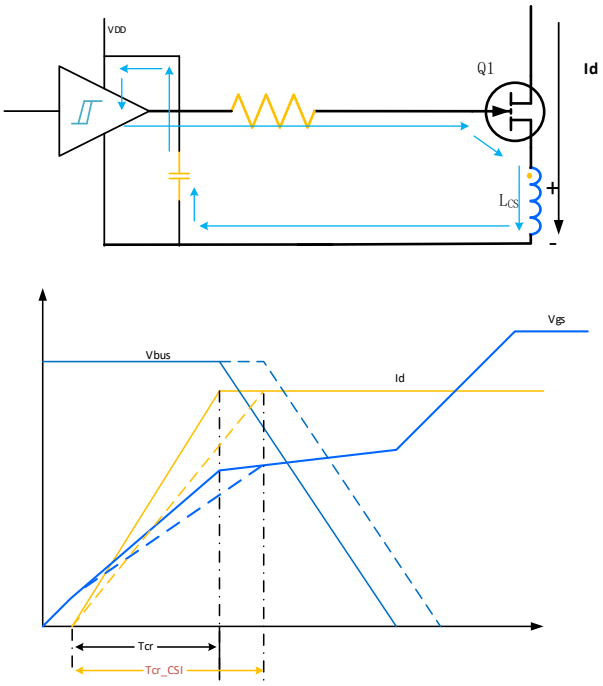


Figure 10 The influence of the common source inductor

During the device turn-on process, the value of di/dt depends on the pull-up/pull-down capability of the driving circuit. With the common source inductor, the drain current slew rate di/dt will generate a negative voltage across the common source inductor during the turn-on process. Therefore the current that charges the gate capacitance is reduced, leads to extended transition time Tcr, increased turn-on losses, and lower efficiency. Attention should be paid to the common source inductor in paralleled InnoGaN design.

3.1.2. Power Loop

Reducing parasitic inductance is crucial for the layout design of high-frequency power devices. The recommended PCB layout design method is as follows:

1.Place MLCC close to the high side InnoGaN. Use the top layer as the power loop forward path while the first inner layer as return path to form the smallest loop size. By this design approach the magnetic fields self-cancellationcould reduce the parasitic inductance in the power loop and benifit to reduce the voltage spikes and improve power efficiency.

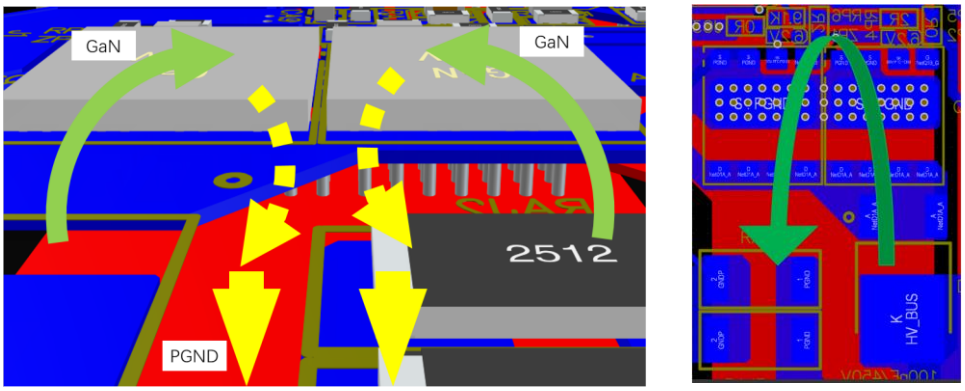
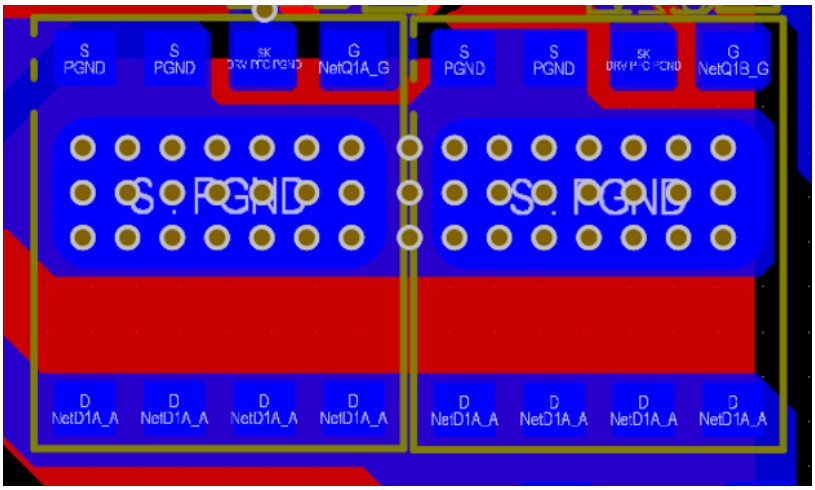


Figure 11 Recommended PCB layout（1）

2. Parallel devices should be symmetrically placed, withthe same number of vias for each device to ensure the same current capability.

Figure 12 Recommended PCB layout（2）



3.1.3. Driving Loop

Based on the driving design guide provided in "AN001 - High-Voltage InnoGaN Driver Design Guide", it is recommended to share the components in driving circuits as much as possible for parallel driving design. Q1A and Q1B share the driving resistors R1 and R2 to ensure the consistency of driving performance. R3 and R4 should be placed near the Gate terminal which could effectively suppresses the ringing caused by the long driving loop. Additionally, the Kelvin design separates the driving loop and the power loop and reduces the effects of CSI (Common Source Inductance)effectively.

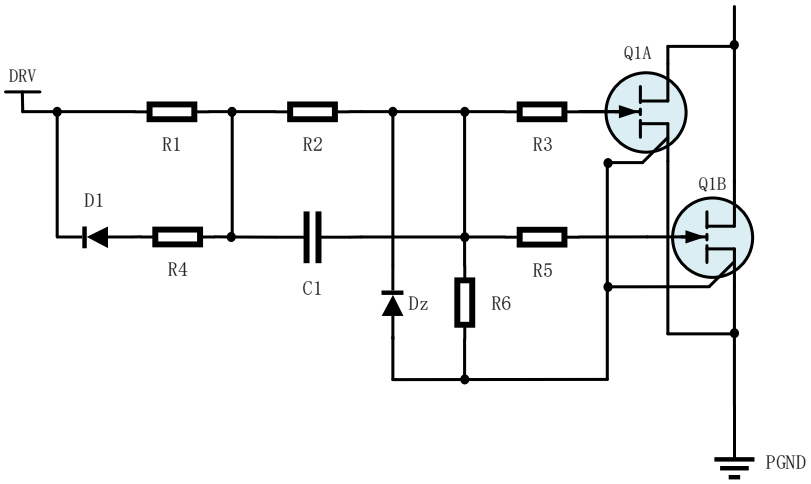


Figure 13 Driving design for paralleled InnoGaN

3.2. Paralleled InnoGaN Design

3.2.1. Parallel InnoGaN Design in Single-FET Topology

Applying paralleled multiple devices in singleFET topologies introduces complexity to the system layout when taken various current paths of each devices into consideration.

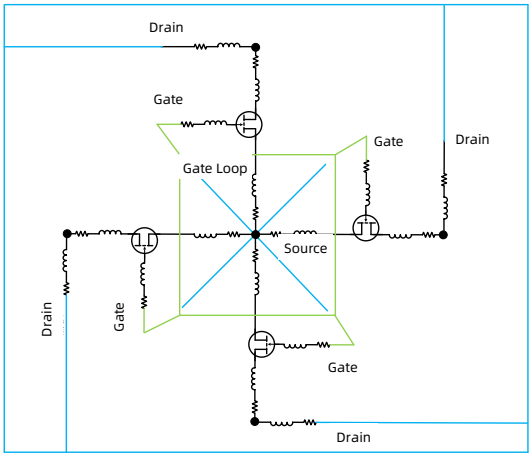


Figure 14 Diagram of Symmetry layout (applicable to high-speed switching applications)

To meet the requirement of symmetry layout of GaN devices, an design example is shown in Figure 12 with the symmetry of the power loop, the common source inductance (CSI), and gate driving loops. As the number of paralleled GaN devices increases, complete symmetry in the layout becomes more difficult to achieve. Therefore, priority should be given as follows:

1.Symmetry in the Common-Source Inductance;

2.Power Loop;

3.Gate Loop;

3.2.2. Paralleled InnoGaN Design in Half-Bridge Topology

Although the layout method for single-FET topologies is also appliable, it may not be the most optimal layout solution for half-bridge topologies. The recommended solution is the mirror symmetry methodas shown in Figure 15.

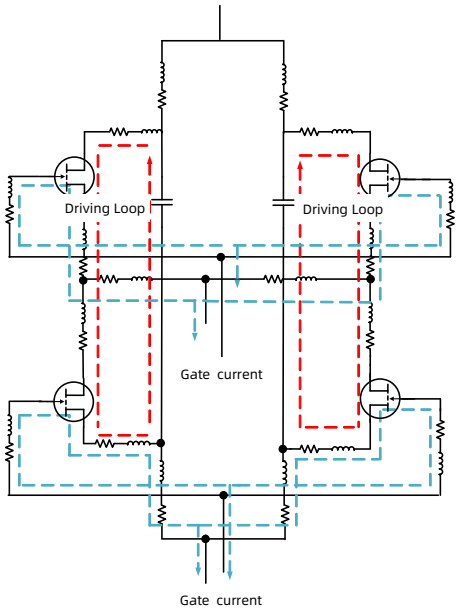


Figure 15 Half-bridge symmetrical layout diagram

The symmetrical scheme realizes a reliable parallel connection for multiple GaN devices in half-bridge topoligies. It features independent power loops, which not only reduce the total loop parasitic parameters but also ensure the consistency of each parasitic parameters, providing the most balanced performance of each device.

4. Design Examples of Paralleled InnoGaN

4.1. Paralleled InnoGaN Design in Low Power PFC

Based on the design considerations in the previous sections, the actual performance is validated in a low power CCM mode PFC circuit. The system employs 2 HV InnoGaN INN650D240A in parallel with the system frequency of 65-100 kHz.

Test conditions: input voltage 90V, PFC output 375V & 0.65A, burn-in 1 hour. The parameters of the paralleled devices are as follows:

Table 2 Measured parameters of paralleled InnoGaN

MPN	Component	Vth(V)	Ron(mΩ)
INN650D240A	Q1A	2.217	156.49
	Q1B	1.508	158.05

4.1.1. Gate Driving Design

According to the design considerations mentioned above, the paralleled GaN FETs share the driving resistors RP1 and RP3 to ensure consistency of gate driving parameters. Additional resistors RP4 and RP5 are employed near the Gate terminal of both GaN FETs to suppress ringing caused by the parasitic parameters in driving loop.

1. Selection of turn-on gate driving resistance: The value of turn-on gate driving resistance depends on parameters such as the Vcc voltage of the controller, gate leakage current, EMI, etc. In this case RP1 is selected as 130Ω.

2. Selection of acceleration capacitor CP1: The acceleration capacitor is used to charge/discharge the Ciss/Crss rapidly. Its value is calculated as follows:

$$CP1 > Qgplat/Vplat \text{ (where } Qg = Qgs + Qgd)$$

According to INN650D240A datasheet, the minimum value of acceleration capacitor should be 720pF, CP1 is chosen as 2.2nF in this case empirically, which is a value 2-3 times larger than the minimum need value.

3. Design Considerations of zener diodes ZP1 and ZP2: Attentions shoule be paid to the parameters such as voltage precision, temperature drift, etc. It

is recommended to use zener diodes with a voltage precision of 2%.

4. The pull-down resistor RP6 is usually selected with between 10-20K empirically.

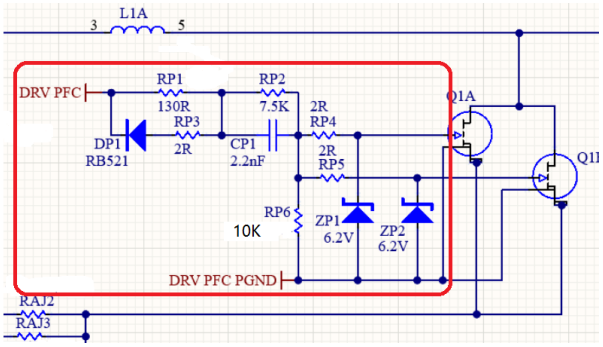


Figure 16 Design Example of Driving Parameters

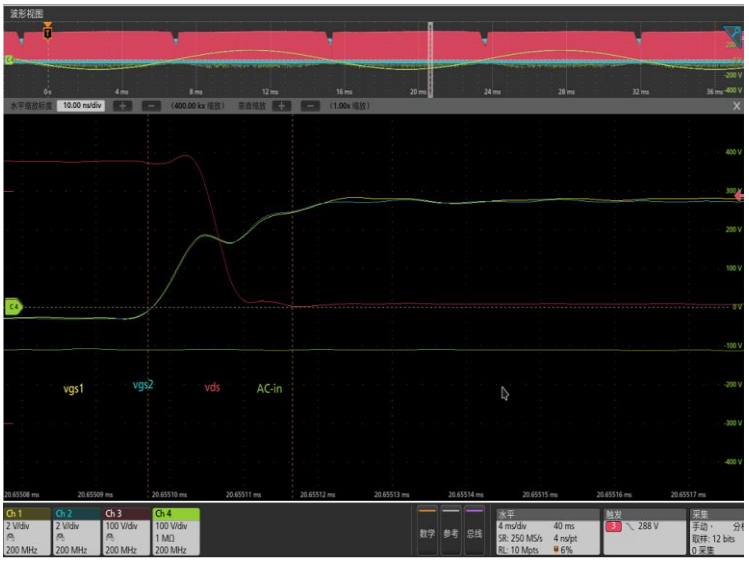


Figure 17 Measured waveforms

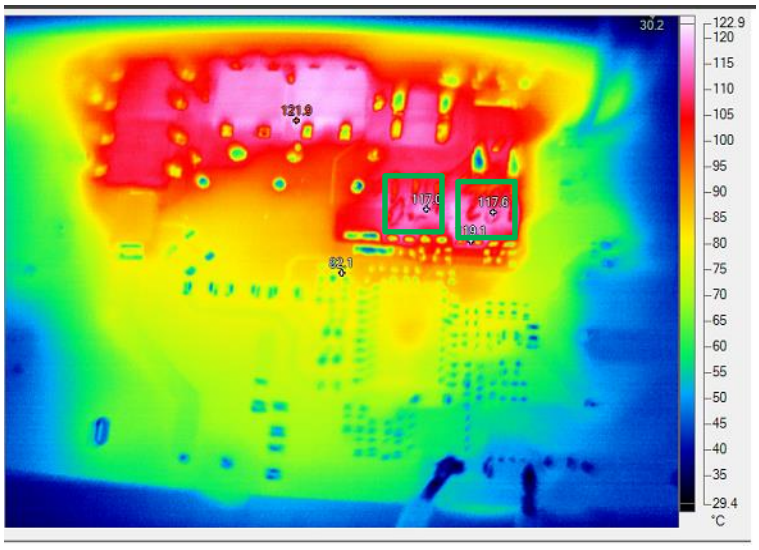


Figure 18 Measured casing temperature

4.1.2. PCB Layout Design

By adopting the following PCB layout, parasitic inductance in the power loop is reduced, while maintaining symmetry in the common-source inductance, minimizing the driving loops, and achieving optimal layout.

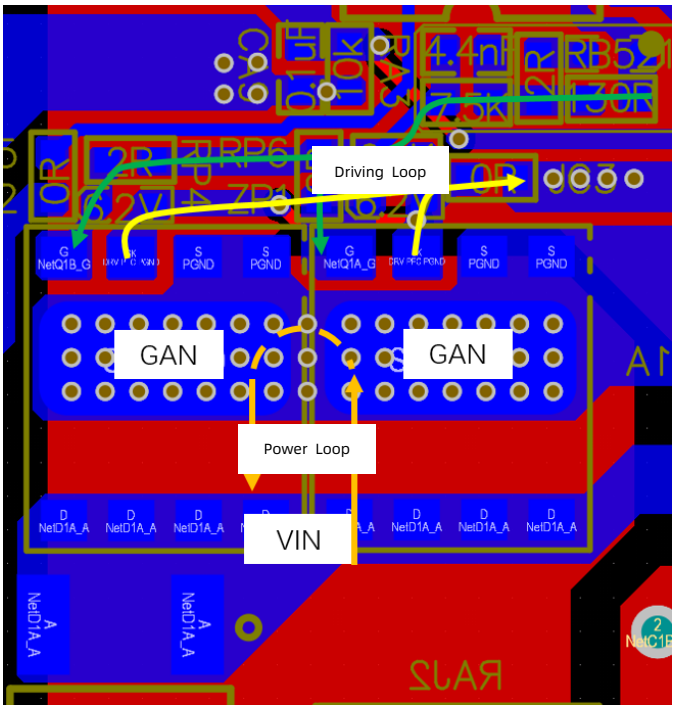


Figure 19 PCB layout design with InnoGaN in DFN8*8

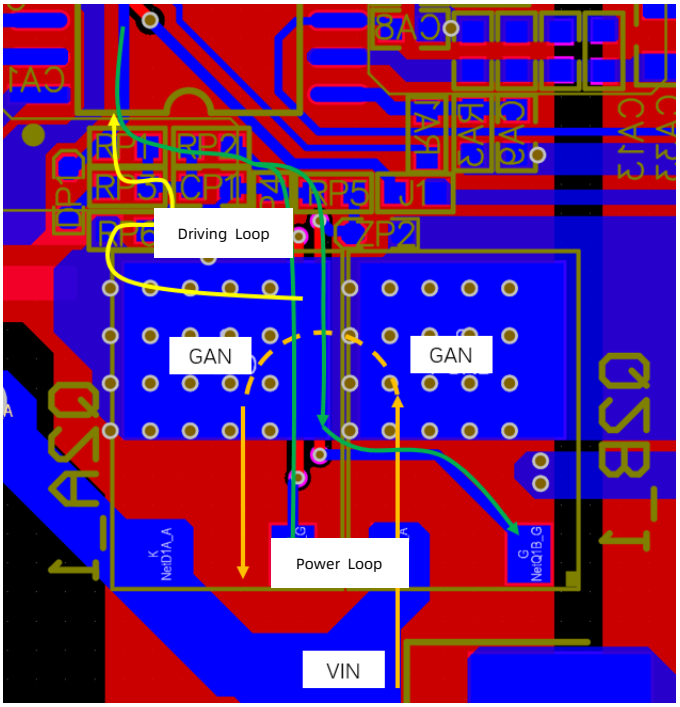


Figure 20 PCB layout design with InnoGaN in TO-252

Revision History

Date	Version	Description	Author
2024/03/29	1.0	English translation	AE team

Note:

There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.

Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:

This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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