POWER THE FUTURE

AN009

App Notes

InnoGaN

Thermal Design Guide

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1. The significance of thermal design

With the development of electronic technology, the eletronic products are becoming increasingly miniaturized. Consequently, the density of electronic compoments on PCB are increasing and the heat flux density of electronic device is also growing. According to the relevant surveys, factors such as temperature, vibration, humidity, and dust are the main cause of failure in power electronic products, with 55% attributed to excessive operating temperature. Once a component in an electronic product reaches a high temperature, it inevitably limits power delivery. In most of the scenarios, the heat generated by switching devices is the limitation factor of power delivery. Therefore, Thermal design is particularly important in power converters.

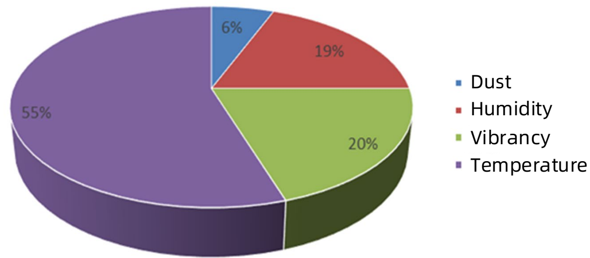


Figure 1 The main factors causing failure in power electronic products [1]

With the device junction temperature(TJ) increases, the RDS(on) of GaN power devices increases, while the transconductance (GM) decreases. The increase of Tj leads to the increase the devices' conduction losses and switching losses, thereby reducing system efficiency. The relation of Tj and power losses is shown as Figure 2.

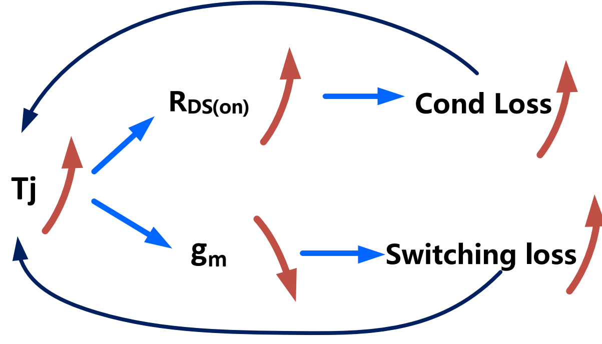


Figure 2 The relationship between Tj and conduction loss and switching loss

2. Cooling and Thermal design

For power supply designers, thermal design of power devices and power systems is critical and sometimes quite challenging. In terms of system-level cooling, considering system cost, various cooling methods such as air cooling, liquid cooling, etc., can be chosen. For complex power systems, regionalization can be employed, distributing different functions reasonably to achieve optimal thermal design. For example, in the design of air ducts, linear air duct design should be used as much as possible to reduce air resistance and maximize heat dissipation. Regarding the heat dissipation of power devices, the main approaches include (1) controlling the internal thermal resistance of the components (junction thermal resistance), which is typically provided in component datasheets, and (2) controlling the external thermal resistance of the components (thermal resistance between the device and air, between the device and PCB, etc.). This paper primarily investigates the influence of external thermal resistance on the temperature rise of the devices.

2.1. The definition of thermal resistance

The term "thermal resistance" refers to the ratio between the temperature difference across an object and the power dissipated by the heat source when heat is transferred through the object. It is measured in Kelvin per watt (K/W) or Celsius per watt (°C/W), and the formula is as follows:

$$R = \frac{\mathrm{T2} - \mathrm{T1}}{\mathrm{P}}$$

In the above equation, T1 represents the temperature at one end of the object, while T2 represents the temperature at the other end of the object, and P is the power dissipated by the heat source (device losses).

Thermal resistance $R_{\theta JA}$: The total thermal resistance from the chip's heat source to the surrounding cooling air.

Thermal resistance $R_{\theta JC}$: The thermal resistance between the chip's heat source and the package outer casing.

Thermal resistance $R_{\theta JB}$: The thermal resistance between the chip's junction and the PCB board.

3. The heat dissipation pathway of GaN device

The heat dissipation pathways for GaN primarily involve bottom-side cooling and top-side cooling. The heat dissipation structures are as follows:

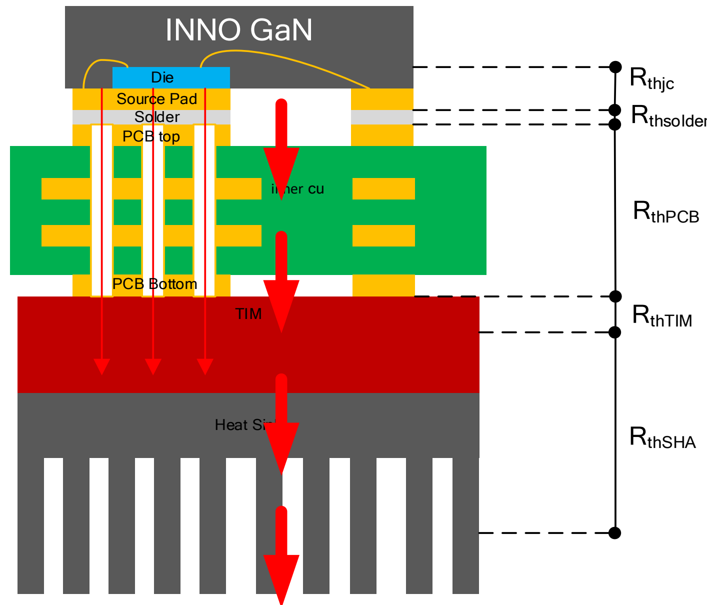


Figure 3 Primary bottom heat dissipation path

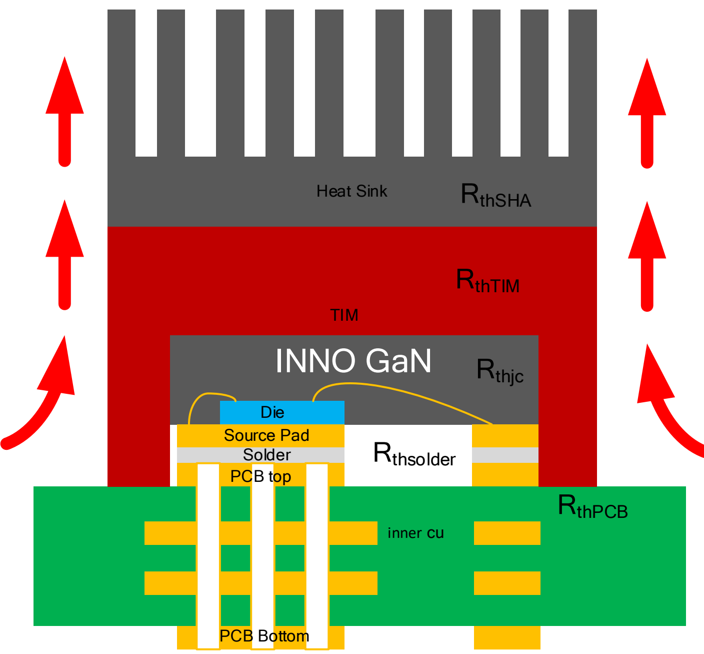


Figure 4 Primary top heat dissipation path

The package of a device significantly influences the selection of the system's heat dissipation pathway.some package is more suibable for bottom-side cooling. For example, as shown in Figure 5, the thermal resistance from the InnoGaN INN650D080BS DFN8*8 package to the solder pad is only 0.52°C/W, making it more suitable for bottom-side cooling.

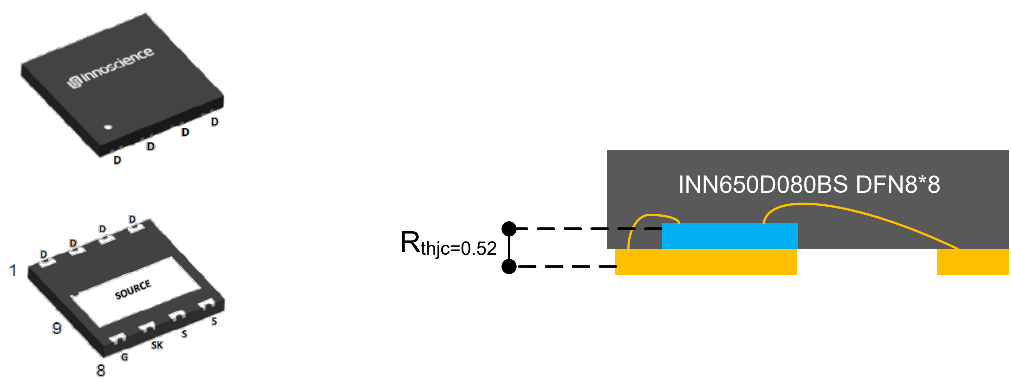


Figure 5 DFN 8x8 The resistance from junction to pad (junction to case)

3.1. The selection of thermal interface materials

Thermal interface materials can fill tiny gaps between devices and heat sinks, increasing the contact area between the device and the heat sink, thereby reducing thermal resistance and further enhancing heat conduction efficiency. It helps to maintain normal temperatures for devices, ensure their proper operation and extending their lifespan.

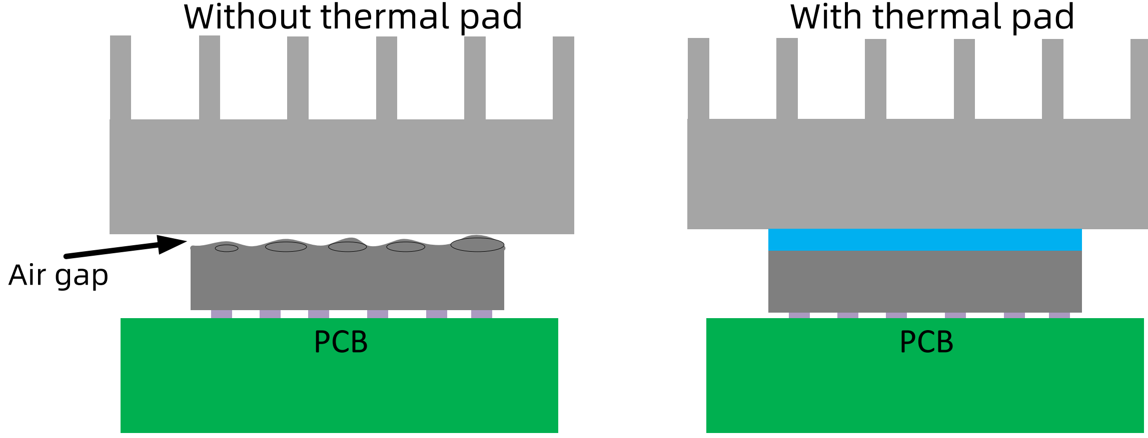


Figure 6 Without or with thermal pad

The selection of thermal interface materials depends on the size of the

gaps to be filled, fixation requirements, the flow characteristics of the material and whether insulation is needed, The table below presents the characteristics and applicable scenarios of commonly used thermal interface materials.

Table 1 Thermal conductive materials

Thermal conductive materials	Picture	Physical property	Application
Thermal grease		High flowability	No insulation requirement, gap size less than 0.1mm, no adhesive needed, alternative fixation measures available
Thermal conductive adhesive		High flow Adhesive	No insulation requirement, gap size less than 0.1mm, adhesive bonding needed
Thermal conductive gel		Midium flowability	Insulation required, 0.25mm < gap < 5mm, no adhesive bonding needed
Thermal pad		No flowability	Insulation required, 0.25mm < gap < 5mm, no adhesive bonding needed, require compression of 30% to 50%

Special attention needs to be paid when using thermal pads as the system pressure requirement should be carefully considered. Generally speaking, the higher thermal conductivity the thermal pads have, the higher hardness it has. Therefore, greater pressure is required to achieve the same compression. It’s necessary to assess the impact of this pressure on the total system.

3.2. Thermal resistance model

No matter which cooling method is used, an equivalent thermal circuit can be used to model the system and analyze its thermal performance. By referring to the device datasheet, one can understand the thermal resistances ($R\theta JC$, $R\theta JB$) of the components. Some thermal resistances vary depending on the system configuration, such as the thermal resistance from the PCB to the environment, $R_{\theta BA}$.

The Buck converter is a common topology in many power electronic circuits. It consists of two transistors, Q1 and Q2, a driver IC, capacitors, and power inductor. The thermal transfer behavior of a discrete GaN Buck power stage is analyzed in the Figure below. This model includes most of the important heat flow paths, with the main heat sources being transistors Q1, Q2, and the power inductor.

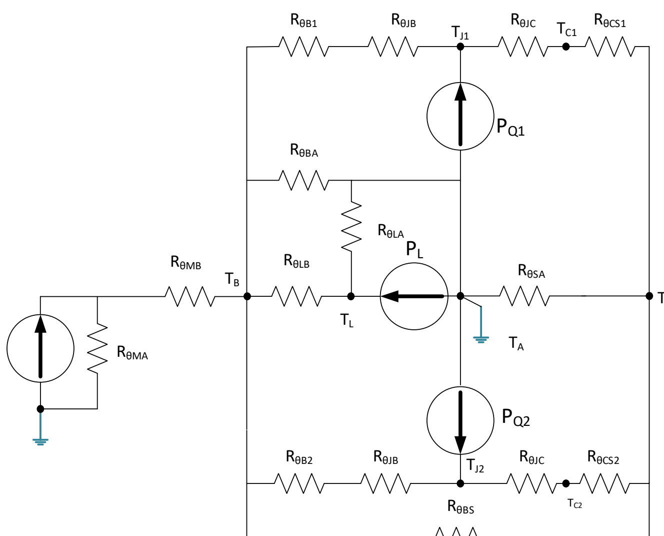


Figure 7. Thermal equivalent circuit for the top-side heat dissipation of the half-bridge power stage

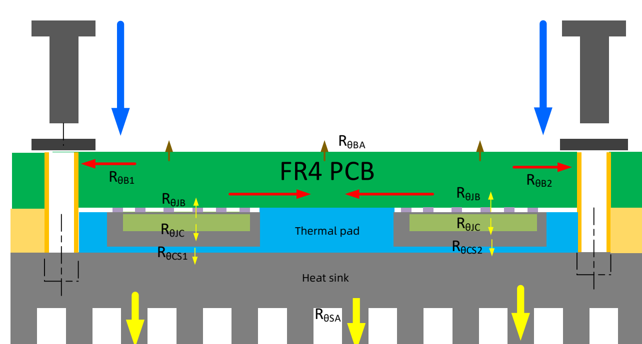


Figure 8. Cross section of half bridge circuit

The temperature node descriptions in this model are defined as follows:

1、 T_{J1} and T_{J2}:Junction temperature inside each GaN device;

2、 T_{C1} and T_{C2}: Case temperatures at the top and side of the substrate of GaN Q1 and Q2;

3、 T_B:Circuit board temperature near the two GaN devices.;

4、 T_S: Heat sink temperature at a single location near the two GaN devices;

5、 T_L: Temperature of the power inductor;

6、 T_A: Temperature around the heat sink;

In this model, thermal resistances represent physical paths as follows:

1、$R_{\theta JC}$: Thermal resistance from the active region of each GaN device to the outer surface of the substrate;

2、$R_{\theta JB}$: Thermal resistance from the active region of each GaN device to the PCB directly below the solder pad;

3、$R_{\theta B1}$、$R_{\theta B2}$:Thermal resistance from the PCB directly below each GaN device to the specified TB position on the PCB;

4、$R_{\theta CS1}$、$R_{\theta CS2}$: Thermal resistance between the substrate of each GaN device and the contact surface of the heat sink (via a thermal interface material);

5、$R_{\theta BS}$: Thermal resistance between TB and the surface of the heat sink;

6、$R_{\theta BA}$: Thermal resistance between TB and the environment;

7、$R_{\theta SA}$: Thermal resistance between the heat sink and the environment;

8、$R_{\theta LB}$: Thermal resistance from the power inductor through the solder pad to the PCB;

9、$R_{\theta LA}$: Thermal resistance from the surface of the power inductor to the environment;

10、$R_{\theta MB}$、$R_{\theta MA}$: Thermal coupling resistances for other system heat transfer through the PCB;

Finally, power dissipation is represented by the following current sources:

1、 P_{Q1} and P_{Q2}: Power dissipation in the GaN devices;

2、 P_L: Power dissipation in the power inductor;

3、 P_M: Power dissipation in other systems on the main board.

3.3. PCB heat dissipation design

The thermal conductivity of copper on PCB boards is 380W/(m*k), while that of FR4 material is 0.3W/(m*k), resulting in a significant difference. Increasing the copper content of PCBs through the use of vias and enlarging copper foil areas can enhance PCB heat dissipation. However, in reality, enlarging the copper coverage and increasing the number of vias are limited by the following factors:

1、 The copper foil area is limited by PCB layout constraints and electrical performance considerations.

2、 Different vias on different packaging types results to different PCB thermal dissipation performance.

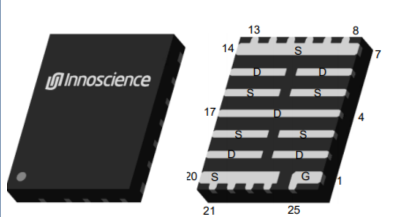
3、 The number of vias affects PCB cost and electrical performance.

Based on above reasons, we need to investigate the PCB via and copper foil thermal design of different packaged devices.

Inno GaN devices have two main types of bottom pad design. Due to differences in bottom pad size and spacing, there are significant variations in design of PCB copper coverage and vias. The following table elaborates on the thermal design for each type of packaging.

Table 2 Two types of bottom solder pad design of InnoGaN device

Package	Example figure	Packaging charateristics	Typical package
Large area of heat dissipation pad		The devices have large-area heat dissipation pads, all of which are source electrodes. During PCB design, it's possible to cover the bottom of the heat dissipation pads with a large area of copper, and it's feasible to place a greater number of vias for additional heat dissipating assistance.	DFN8*8 DFN5*6 TOLL FCLGA TO-252

Interleaved bottom heat dissipation pads		The devices have drain and source electrodes arranged in an interleaved manner with small space, making it impractical to cover a large area with copper on the bottom of the heat dissipation pads. Additionally, due to the limited area of the pads, there are fewer vias for thermal dissipation on the bottom.	FCQFN EN-FCQFN FCLGA WLCSP

3.4. Summary

This chapter introduces basic definitions of thermal resistance and thermal models, along with the fundamental structures of bottom-side and top-side heat dissipating.

Additionally, it discusses the characteristics and applicable scenarios of several commonly used thermal interface materials. The PCB heat dissipating design for InnoGaN is categorized into two main types based on different bottom pads. The design of the two main types will be discussed in detail in subsequent chapters.

4. The package with large-area heat dissipation pad of thermal design

4.1. The package design with large-area heat dissipation

4.1.1. The impact of via on solder pads

The main impact of vias on heat dissipation is the effect of the copper content per unit area on the thermal resistance of the PCB. The higher copper content, the lower thermal resistance of PCB. However, the smallest distance between the edges of vias (>0.2mm)is limited by the processing technology. The effects of vias inside the solder pad on thermal resistance for DFN8*8 and TOLL packages are shown as follows:

DFN8*8

The test samples are divided into two groups: A, and B. Each group uses via diameters of 0.3mm and 0.4mm, with different edge-to-edge via and center-to-certer via distances, shown as Table 3.

Table 3 The solder pad and parameter of package DFN 8*8

	A1	A2	A3	B1	B2	B3
Via diameter(mm)		0.3			0.4	
Via edge to edge(mm)	0.45	0.7	1.2	0.45	0.6	1.1
Via center to center(mm)	0.75	1	1.5	0.85	1	1.5

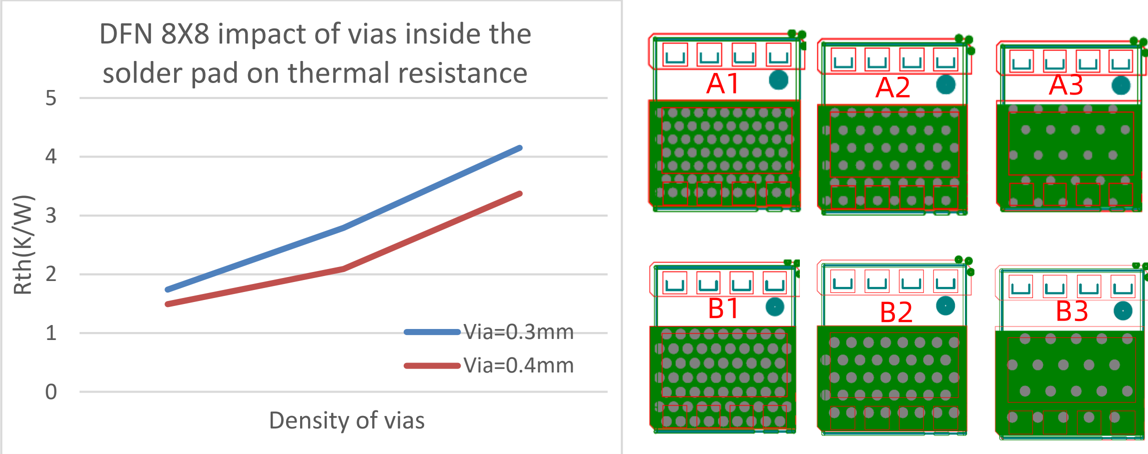


Figure 9 The parameters of the DFN8*8 solder pad and the impact of vias inside the solder pad on thermal resistance

It can be observed that the more vias inside the bottom solder pad, the lower thermal resistance. The thermal resistance of A1 is 58% lower compared with A3. For DFN8*8 package, using a via diameter of 0.4mm results in the

lowest thermal resistance, with a 15% reduction compared to 0.3mm vias.

It is recommended to use 0.4 diameter vias with a center-to-center distance of 0.85mm for DFN8*8 devices (B1 configuration).

TOLL

Table 4 The solder pad and size parameters of TOLL package

	A1	A2	A3	B1	B2	B3
Via diameter(mm)	0.3			0.4		
Via edge to edge(mm)	0.45	0.7	1.2	0.45	0.6	1.1
Via center to center(mm)	0.75	1	1.5	0.85	1	1.5

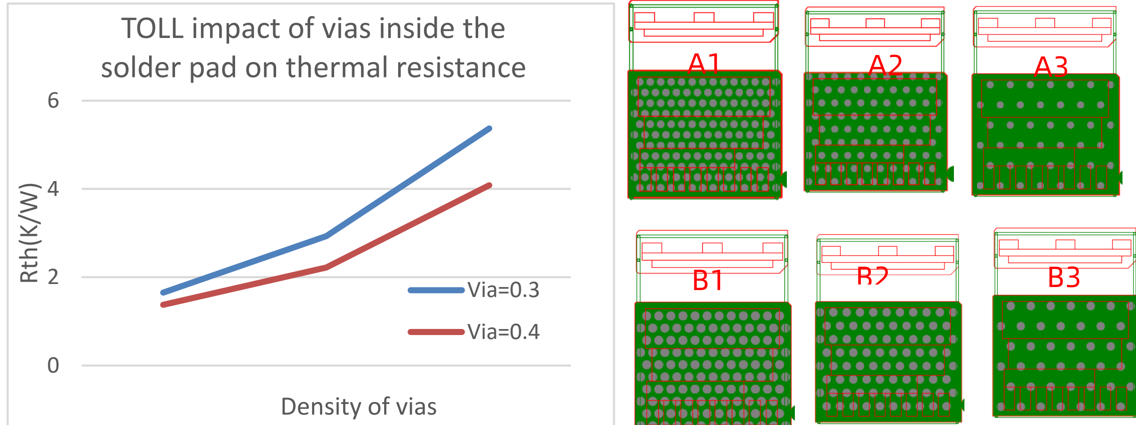
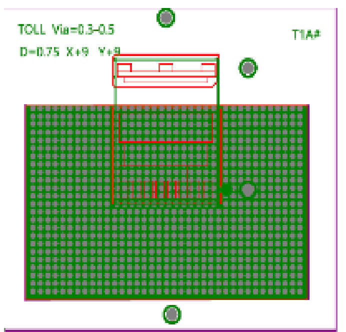


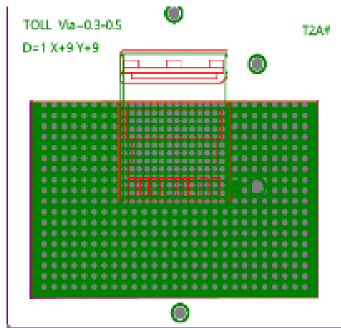
Figure 10 The parameters of the TOLL solder pad and the impact of vias inside the solder pad on thermal resistance

For TOLL packages, using a via diameter of 0.4mm results in the lowest thermal resistance, with a reduction of 16.5% compared to using 0.3mm vias. It is recommended to use 0.4/0.6mm vias with a center-to-center distance of 0.85mm for TOLL package devices.

4.1.2. The impact of outer vias on thermal resistance

The effect of the number of outer vias on PCB thermal resistance is tested for TOLL packages. Inner vias have a diameter (ID) of 0.3mm and an outer diameter (OD) of 0.5mm, with a spacing of 0.75mm between vias. Same-size vias are placed outside the solder pad area, on a copper-covered area measuring +9mm in the X direction and +9mm in the Y direction relative to the package. The spacing between outer vias is varied from 0.75mm to 1.5mm to evaluate the impact of the number of peripheral vias on PCB thermal resistance.





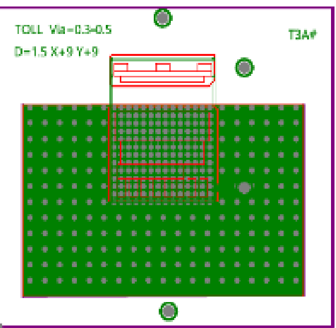


Figure 11 Test schematic illustrating the effect of the number of outer vias on PCB thermal resistance

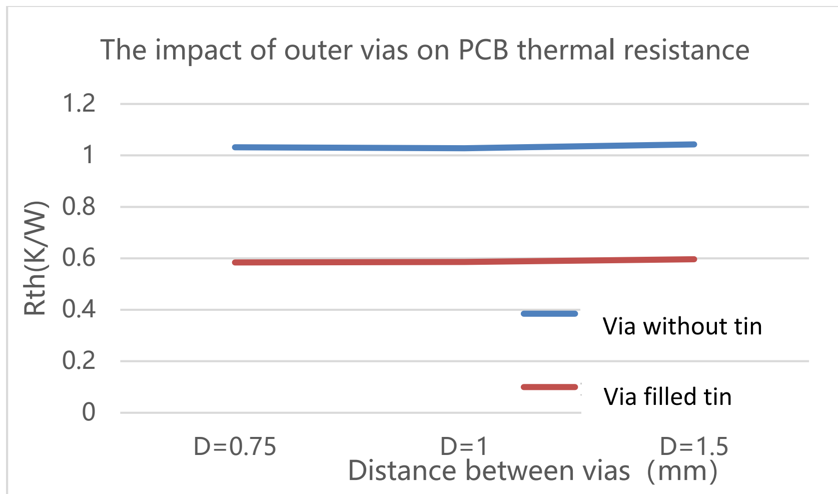


Figure 12 The effect of the number of outer vias on PCB thermal resistance

From the test results, it can be concluded that the number of peripheral vias has a minimal impact on PCB thermal resistance. With the via spacing varying from 0.75mm to 1.5mm, the thermal resistance only changed by 0.02K/W.

4.1.3. The impact of outer copper foil on heat dissipation

The inner vias are the same as described in section 3.1.2. However, the outer copper foil area surrounding the solder pads is varied. The copper foil area increases from X direction +2mm Y direction +2mm to X direction +8mm Y direction +8mm. The change in PCB thermal resistance is tested.

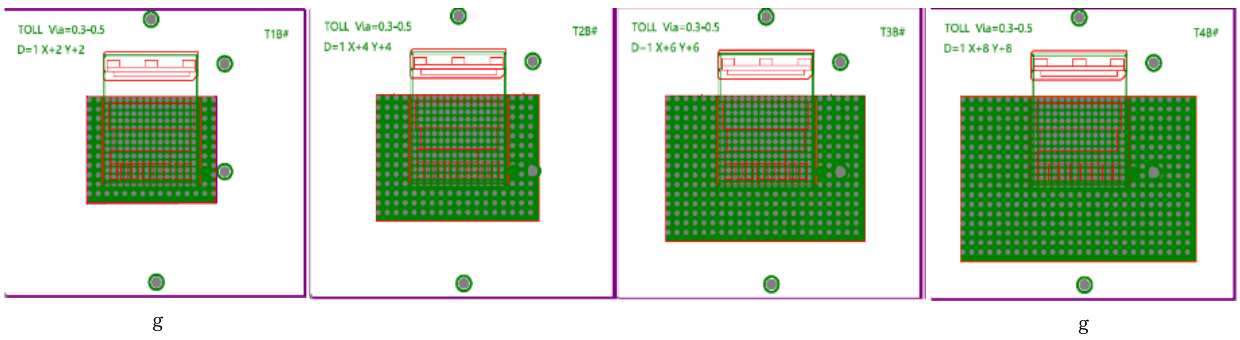


Figure 13 Test schematic illustrating the impact of outer perimeter copper foil area on PCB thermal resistance

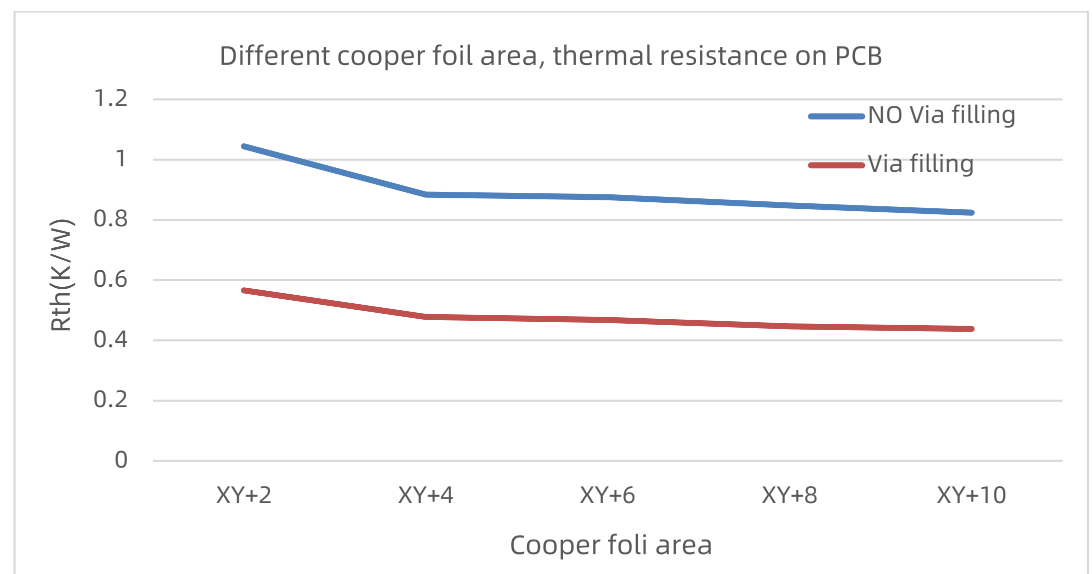


Figure 14 The impact of outer perimeter copper foil area on PCB thermal resistance

From the test results, it can be observed that the copper foil from XY+2 to XY+4 has a significant impact on PCB thermal resistance. The thermal resistance at XY+2 decreased by 37%, while at XY+4, it decreased by 16% compared to XY+2. Further enlargement of the copper foil area resulted in diminishing returns. Therefore, for an effective PCB thermal design, it is recommended to ensure a minimum copper foil area of XY+4 for heat dissipation.

4.1.4. The impact of PCB thickness on thermal resistance

According to the test results, PCB thickness directly affects its thermal resistance. The thermal resistance of a 1mm PCB is 40% lower compared to a 2mm PCB

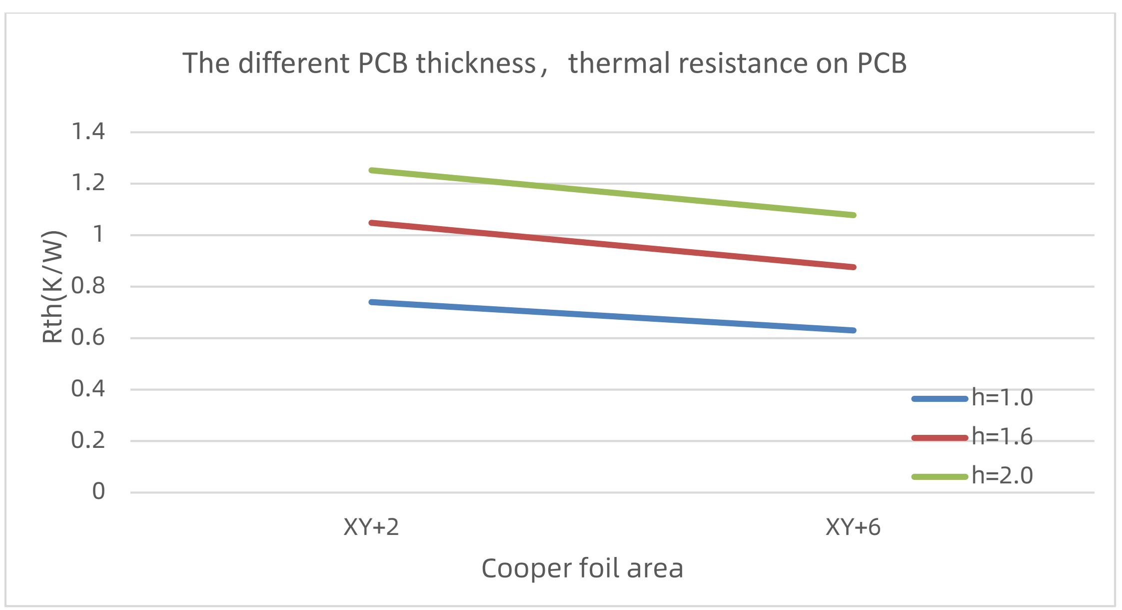


Figure 15 The impact of PCB thickness on thermal resistance

4.1.5. Summary of bottom PCB heat dissipation design

1、 The more vias at the bottom of device solder pads, the lower PCB thermal resistance. For DFN8*8 and TOLL packaged devices, using vias with an inner diameter of 0.4mm and a via pitch of 0.85mm results in the lowest PCB thermal resistance.

2、 When there are numerous vias within the solder pads, the quantity of vias around the periphery has minimal impact on PCB thermal resistance.

3、 Copper foil around the solder pads, ranging from 2mm to 4mm, significantly affects PCB thermal resistance. Further increasing the copper foil area yields diminishing returns.

4、 PCB thickness directly affects thermal resistance. Please prioritize using thinner PCB materials while ensuring structural integrity

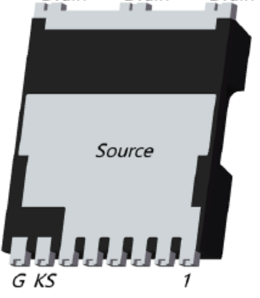
4.2. Application instance

4.2.1. Application in TOLL package of thermal design

A 4KW Totem Pole PFC utilizing Inno GaN INN650TA030AH (650V 30mΩ) devices is studied as an application example, with the following device specifications:

Table 5 INN650TA030AH device parameters

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$ @ V_{GS} = 6 V	34	mΩ
$Q_{G,typ}$ @ V_{DS} = 400 V	16	nC
$I_{D,pulse}$	100	A
Q_{oss} @ V_{DS} = 400 V	200	nC
Q_{rr} @ V_{DS} = 400 V	0	nC



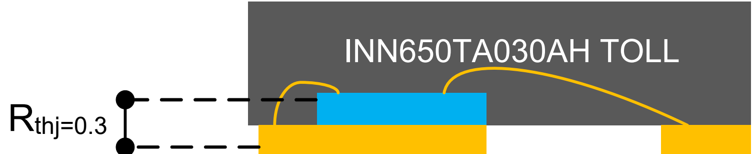


Figure 16 INN650TA030AH device schematic diagram

The TOLL package structure has a thermal resistance (Rthjc) of only 0.3℃/W at the bottom solder pads, making it more suitable for bottom heat dissipation.

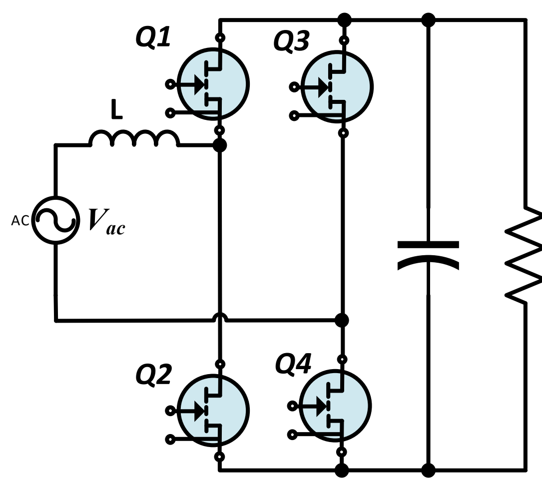


Figure 17 The 4kW totem pole bridgeless PFC topology

(a) Top Layer	(b) Mid Layer 1
(c) Mid Layer 2	(d) Bottom layer

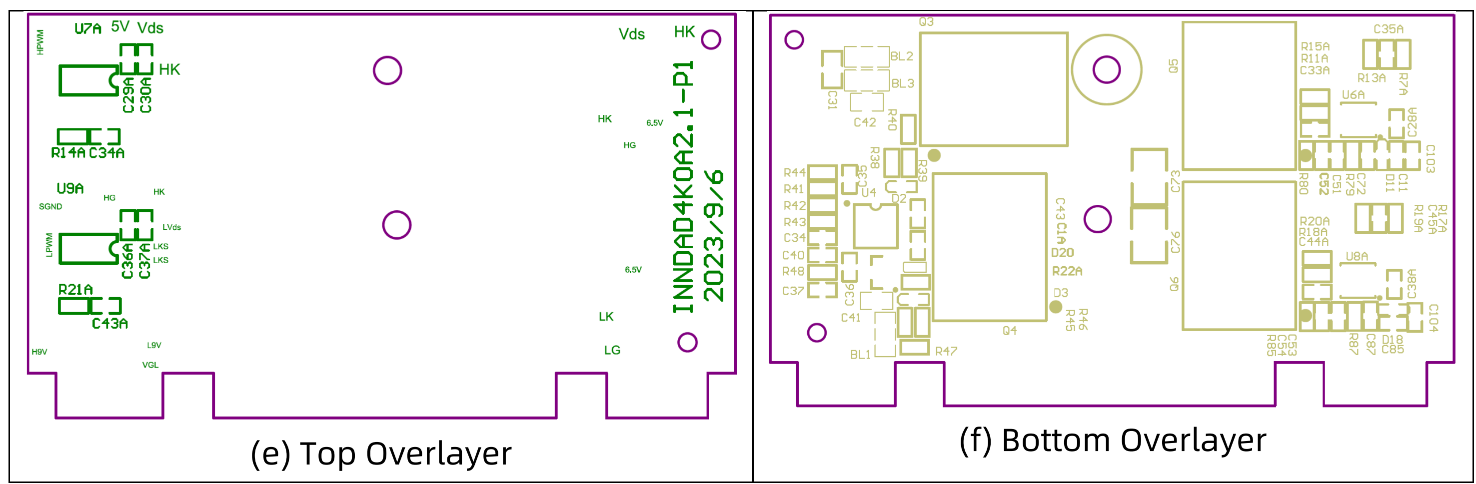


Figure 18 Design of 4kW totem pole bridgeless power factor correction PCB

Thermal design:

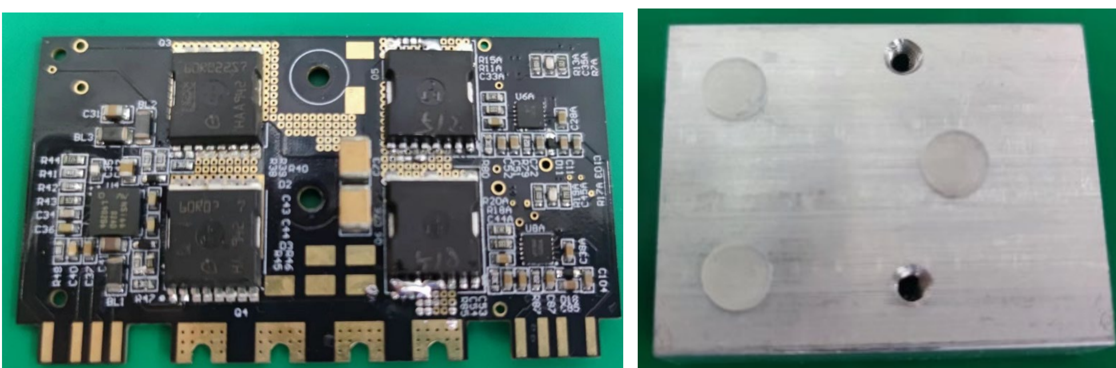


Figure 19 Physical map of thermal design

1、 Attach a 1mm thick silicone pad to the heatsink.

2、 Apply thermal conductive with model number XK-40S(Glpoly, thermal conductivity:4W/m*/k)on the PCB.

3、 Secure the heatsink to the PCB using screws.

4、 Heatsink specifications:20*30*15mm;PCB specifications: PCB thickness 1mm, component solder pad via hole 0.4/0.6, hole spacing 0.85; copper thickness 2oz.

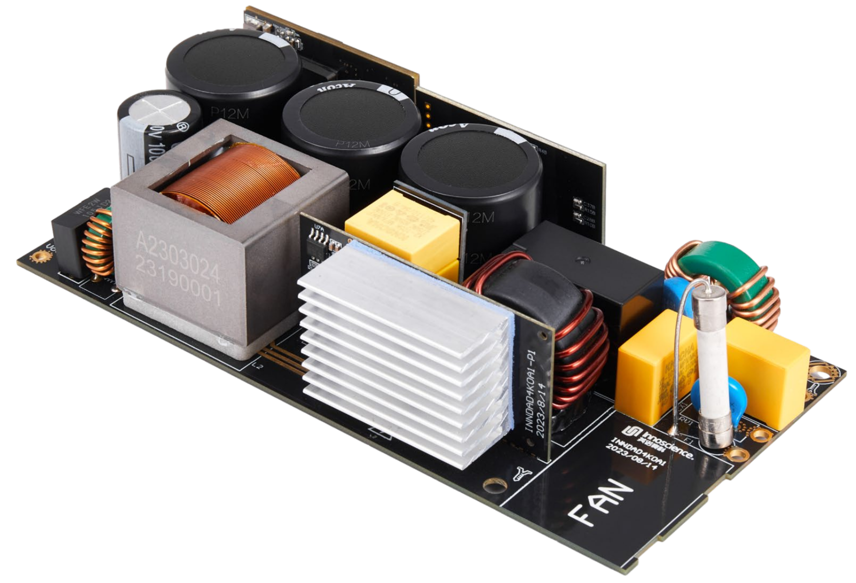


Figure 20 4KW totem pole PFC

Under conditions of Vin=230Vac, Po=3.9KW, and fan power of 15W, the temperature of the high side and low side Inno GaN transistors was measured at 67.4℃ and 71.4℃ respectively.

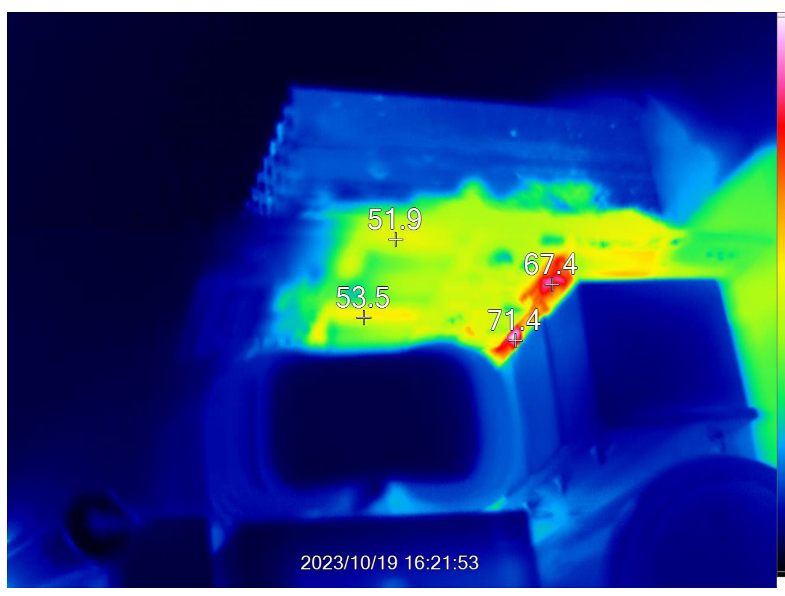


Figure 21 Thermal imaging testing of 4KW PFC demo

5. Interleaved bottom solder pad thermal design

5.1. Interleaved bottom solder pad PCB design

5.1.1. The impact of vias on GaN heat dissipation

This section analyzes the conditions with PCB dimensions: 50mmx50mm, and the copper area of the PCB as 1S=6.25mmx6.25mm. The device evaluated is INN030FQ015A, with $R_{\theta JB}$: 1.5℃/W, and $R_{\theta JC}$: 12.4℃/W. The device is positioned in the middle of the PCB, with a power loss of 1W. The PCB thickness is uniformly 1.6mm with a copper thickness of 2oz, and it's a 4-layer board. Only the heat-generating devices INN030FQ015A is mounted on the PCB board. The analysis scenario assumes no airflow. The $R_{\theta JA}$ in Table 1 is obtained on a one square inch FR4 board, single layer with 2oz copper.

Table 6 The thermal resistance information for the device INN030FQ015A

Symbol	Paratemer	Typ	Unit
$R_{\theta JC}$	Thermal Resistance，Junction to Case	12.4	℃/W
$R_{\theta JB}$	Thermal Resistance，Junction to Board	1.5	℃/W
$R_{\theta JA}$	Thermal Resistance，Junction to Ambient	54.5	℃/W

The relationship between device heat dissipation and vias is significant in PCB design. Vias not only carry current between different layers but also ensure a heat dissipation path for devices. Here are some aspects of the relationship between device heat dissipation and Vias:

1、 Via positioning: Under the same PCB area (12.5mm x 25mm), the impact of different Vias positions on device thermal resistance is compared. This analysis examines four scenarios: via design directly above the solder pad, near the solder pad, 1.4mm away from the solder pad side, and 5.8mm away from the solder pad side. A comparison of the device temperature rise is made under the same power dissipation (1W for both upper and lower transistors).

Table 7 The analysis of different via position to the device thermal resistance

	Option 1 On the pad	Option 2 Near the pad	Option 3 1.4mm away from the solder pad side	Option 4 5.8mm away from the solder pad side
Thermal resistance (℃/W)	113.2	115.5	116.3	116.9
PCB				

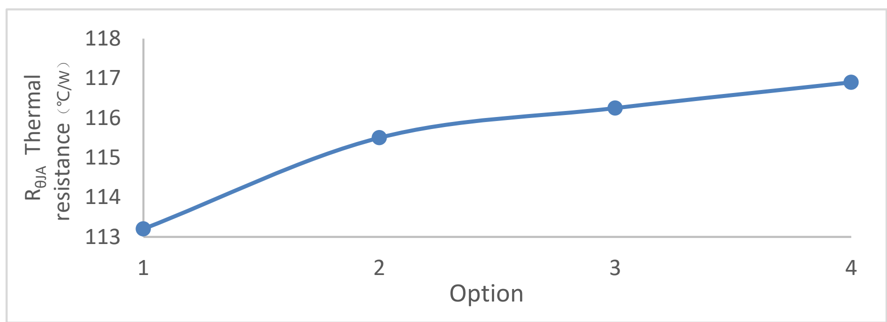


Figure 22 The analysis of different PCB layout to the thermal resistance

From the data, it can be observed that as the via moves away from the device solder pad, its thermal resistance increases, leading to poorer heat dissipation. Therefore, it's recommended to prioritize placing the vias directly on the device's solder pad.

2、 Vias quantity: With a copper area of 4S, the impact of the number of vias on heat dissipation is studied. Excessive vias numbers can increase the local impedance of the PCB, affecting the efficiency of current transmission. Selecting the appropriate number of vias is crucial for system efficiency and thermal management.

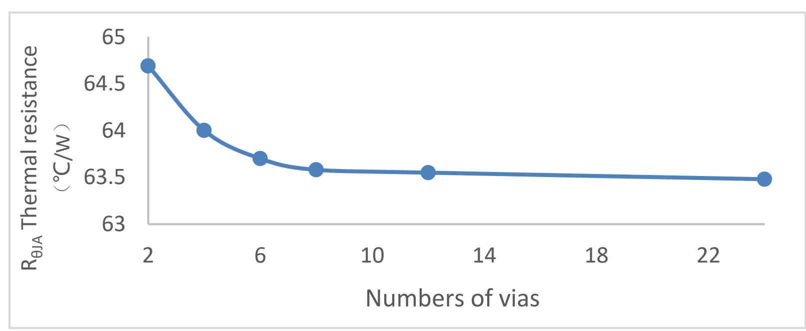


Figure 23 The relationship between vias and thermal resistance

Analyzing the data reveals that when the number of vias increases to 6, there is little change in system thermal resistance. Therefore, it is recommended to have 6 vias per solder pad, provided that the via current density requirements are met.

3、 Via distance: With a copper area of 4S, the impact of different via distance (distance between the centers of two vias) on heat dissipation is studied. Due to the dimensions of the device (INN030FQ015A) solder pads, it is generally recommended to have via parameters of 0.3mm/0.2mm. A comparison of thermal resistance variations for different via distance with 6 vias per solder pad is as follows.

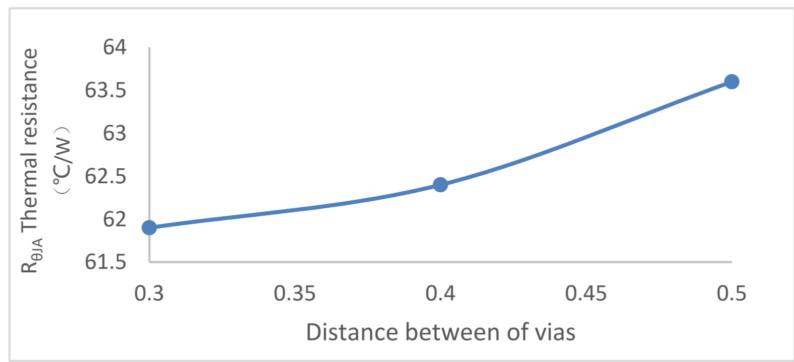


Figure 24 The relationship between vias distance and thermal resistance

It's evident that larger via distance results in higher thermal resistance, affecting device heat dissipation. Therefore, it's preferable to prioritize combinations with smaller distance, provided mechanical stress isn't compromised.

4、 The impact of via filling on device heat dissipation. To improve thermal conductivity in the board thickness direction,vias' walls are copper-plated, effectively acting as a conduit to transfer heat from

one side of the device to the other, enhancing device heat dissipation. Vias typically consist of hole walls and filling materials. Analyzing and comparing thermal resistances for different filling materials, it's observed that using copper filling can help reduce thermal resistance and enhance device heat dissipation. Analysis indicates that, under conditions where cost allows, filling vias with copper can enhance heat dissipation while reducing the vias' own heat generation.

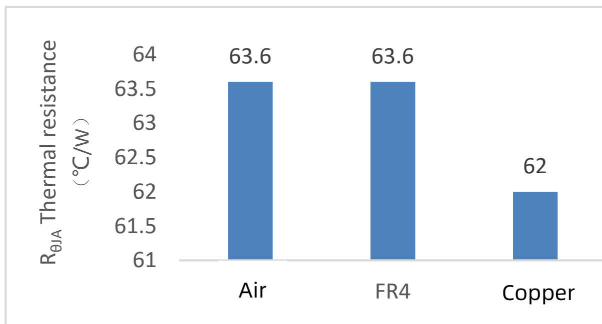


Figure 25 The relationship between filling vias and thermal resistance

Based on the above analysis, there's a correlation between device heat dissipation and via distance. In PCB design, it's crucial to consider factors such as the number, position, size, and cost of vias to optimize heat dissipation. Additionally, it's essential to integrate specific heat dissipation designs to ensure the normal operation of devices.

5.1.2. The impact of PCB area on GaN heat dissipation

Due to the constraints imposed by PCB layout routing, it's not feasible to flood copper everywhere. Hence, it's crucial to find a well-balanced point. Quantitative analysis is conducted by varying the copper foil area under different scenarios: 2S/4S/6S/8S/12S/16S.

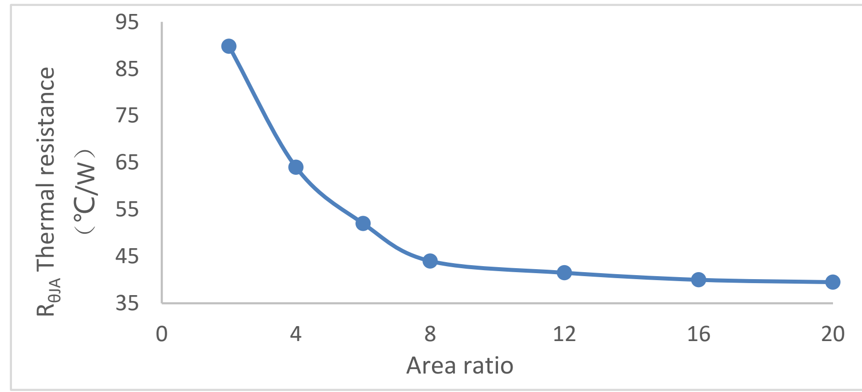


Figure 26 The impact of PCB area on thermal resistance

The thermal resistance undergoes the most significant change before reaching 8S. Within the limited board space, to minimize device temperatures, it's advisable to increase the copper area beneath the chip moderately, with 8S as the maximum limit.

5.1.3. The impact of PCB layers on GaN heat dissipation

In PCB production design, the mainstream printed circuit board material is FR-4. Due to FR-4's low thermal conductivity, heat transfer on the circuit board primarily relies on copper foil. This section investigates the influence of PCB layers. Thermal resistance data is compared and analyzed for PCB layers of 2/4/6/8, with a copper foil area of 4S. More PCB layers are beneficial for device heat dissipation.

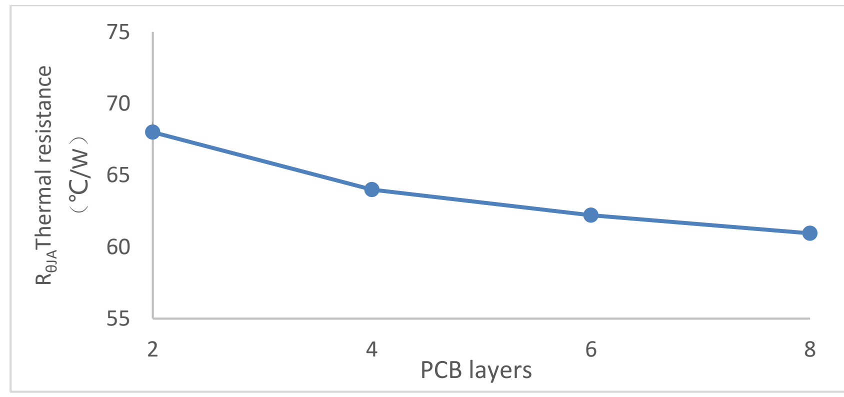


Figure 27 The relationship between thermal resistance and PCB layers

5.1.4. Summary of heat dissipation design for package with interleaved bottom pads on PCB

Factors affecting GaN heat dissipation in PCB design, including layer stacking, routing, copper placement, and vias, must be carefully considered during the design process. Specific design guidelines are outlined as follows:

PCB via design:

1、 It is recommended to have a minimum of 6 vias per pad, ensuring sufficient current density support.

2、 For specific via diameters (0.3mm/0.2mm), maintain a via-to-via spacing of 0.3mm for optimal heat dissipation.

3、 Under the same via quantity condition, prioritize placing vias directly beneath the pads for enhanced thermal performance.

Layer stacking:

1、 In a PCB board, lateral thermal conductivity is stronger than vertical conductivity, influenced by copper foil and FR-4 material properties. When feasible, consider increasing copper thickness on the heat-emitting surface.

2、 If cost permits, consider adding more layers to the PCB and this aids in reducing device temperature rise.

Cooper foil positioning and area:

1、 When designing the PCB, ensure that copper foil extends in every direction from the device ground. If possible, surround the device with copper, centered around the device.

5.2. Application example

5.2.1. Application example of QFN package

The experiment data testing was conducted on a buck topology with four parallel INN030FQ015A[2] half-bridge configurations. The device specifications are as follows:

Table 8 INN030FQ015A device parameters

Parameter	Value	Unit
$V_{DS,max}$	30	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	1.5	mΩ
$Q_{G,typ}$ @ V_{DS} = 15 V	22.8	nC
$I_{D,pulse}$	300	A
Q_{oss} @ V_{DS} = 15 V	43	nC

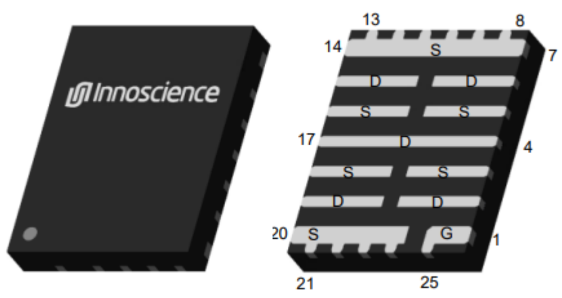


Figure 28 INN030FQ015A device schematic

The topology diagram is as follows:

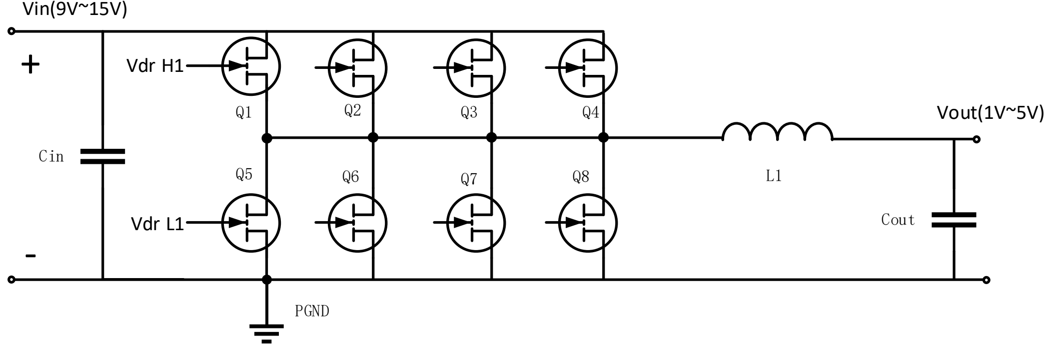


Figure 29 Topology schematic

(a) Top Layer

(b) Mid Layer 1

(c) Mid Layer 2

(d) Bottom layer

(e) Top Overlayer

(f) Bottom Overlayer

Figure 30 The PCB design of paralleled four hemts buck

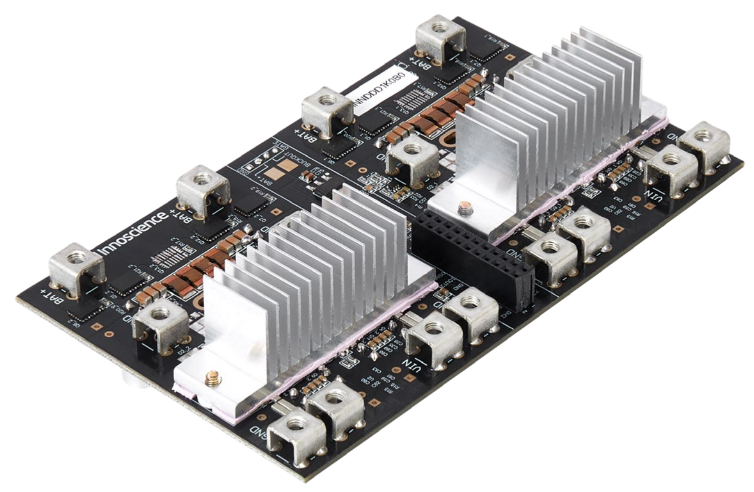


Figure 31 The photo of two interleaved four hemts parallel buck configuration

Figure 32 Thermocouple test point

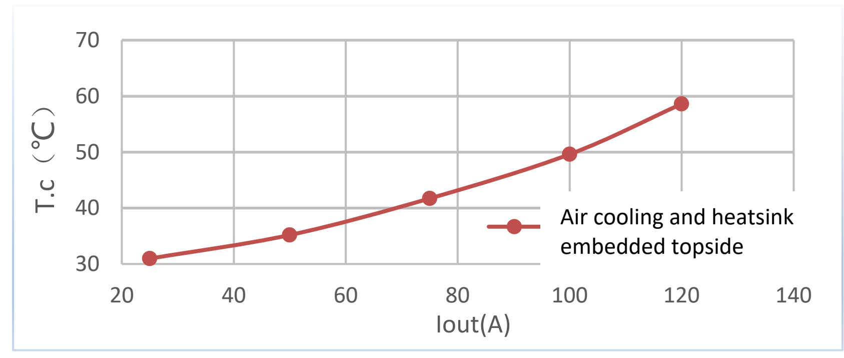


Figure 33 Temperature testing of thermocouple under different loads

The system PCB utilizes an FR4 4-layer board with a thickness of 1.6mm and copper thickness of 2oz. The system operates at a frequency of 300kHz with Vin at 12V and Vout at 5V. The thermal pad used is NDST-CP120-T500-T1, with a thermal conductivity of 5W/(m*K). With an output of 120A, the system was tested with a thermocouple, yielding a temperature of 58.6°C, indicating good thermal dissipation performance.

Reference

1、 Yang, Z., Zhang, Z., Quan, P., Xia, D., & Liu, Z. (February 2020). Thermal Analysis and Thermal Design Optimization of Photovoltaic Grid-connected Inverters Based on Icepak. Journal of Solar Energy, Vol. 41, No. 2.;

2、 https://ynsk.shwebspace.com/uploads/INN030FQ015A_Datasheet_Rev1.0_20231227.pdf

Reversion History

Date	Version	Description	Check
2024/04/12	1.0	English translation	AE team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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