Innoscience 英诺赛科

POWER THE FUTURE

AN002

Application Note

LV InnoGaN

Gate Driving Design Guide

List of Contents

1. Introduction of InnoGaN gate driving characteristics

1.1. InnoGaN structures

Figure 1 illustrates the schematic structure of InnoGaN, which is a GaN HEMT with p-GaN enhanced gate. When the built-in voltage generated by the p-GaN structure exceeds the voltage induced by the AlGaN/GaN heterojunction beneath it, the two-dimensional electron gas (2DEG) under the gate is depleted, forming an enhanced gate. The p-GaN structure can be considered as a pair of Schottky junction and a PN junction back-to-back in series connection. Currently, the maximum long-term positive gate bias voltage for low-voltage (LV) InnoGaN products is 6V. For detailed gate voltage ratings, please refer to product datasheets. The specifications for LV InnoGaN can be found on **Innoscience website – Products**.

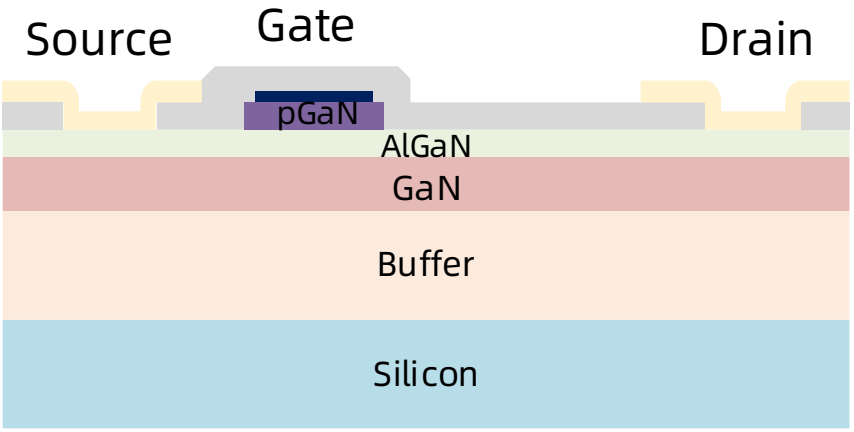


Figure 1 Schematic Diagram of LV InnoGaN Structure

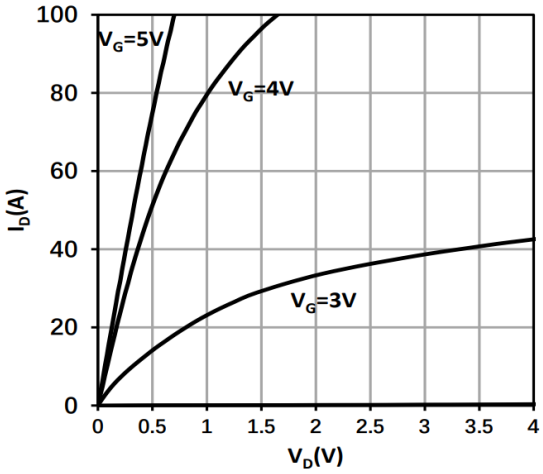
1.2. Gate Characteristics of LV InnoGaN

Due to the inherent characteristics of p-GaN, the maximum gate-to-source voltage (V_{GS}) of LV InnoGaN is 6V, while the reverse V_{GS} rating is -4V, as shown in **Table 1**. Attention should be paid to the selection of driving voltage and layout design to avoid overvoltage in the design procedures.

Table 1 Key Parameters of LV InnoGaN

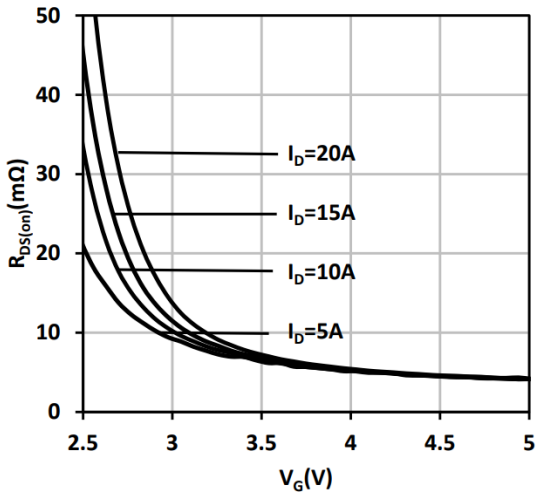
Symbol	Parameter	Max	Unit
V_{DS}	Drain-to-Source Voltage（Continuous）	100	V
I_D	Continuous current	60	A
	Pulsed（25℃, TPULSE = 300us）	230	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	℃
T_{STG}	Storage Temperature	-40 to 150	℃

Figure 2 and Figure 3 show the V_{GS}-I_D curve and V_{GS}-$R_{DS(on)}$ curve of the INN100W032A, respectively. In practical applications, it is generally recommended to use a higher gate driving voltage within the V_{GS} voltage rating to ensure optimal performance of InnoGaN. This enables the system to achieve higher load capacity and efficiency. A gate driving voltage of 5V is typically recommended for LV InnoGaN products.



$I_D = f(V_D, V_G)$; T_J = 25 °C

Figure 2 V_{GS}-I_D curve



$R_{D(on)} = f(V_G, I_D)$; T_J = 25 °C

Figure 3 V_{GS}-$R_{DS(on)}$ curve

1.3. Comparison between InnoGaN and Si MOSFETs

- **Similarities:**

1、 InnoGaN and e-mode Si MOSFETs are both normally-off power devices.

2、 Both are voltage-driven, where the driver IC charges and discharges the parasitic capacitances (C_{ISS} and C_{RSS}) of the device, and provides the gate leakage current (I_{GSS}) during positive bias.

3、 The switching speed can be adjusted with an external gate resistor (R_{g_ext}).

- **Differences:**

1、 Gate voltage rating and threshold voltage (V_{th}): InnoGaN has lower gate voltage tolerance and threshold voltage, requiring a smaller driving loop to reduce interference.

2、 Driving Voltage: The recommended gate driving voltage for LV InnoGaN is 5V, which is lower than the 8-12V for Si MOSFETs. If compatibility with controllers for Si MOSFETs is needed, the driving voltage of the controller must be stepped down, or an additional driver IC should be used to meet voltage requirements for InnoGaN.

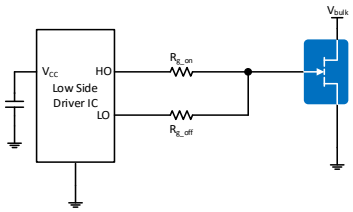
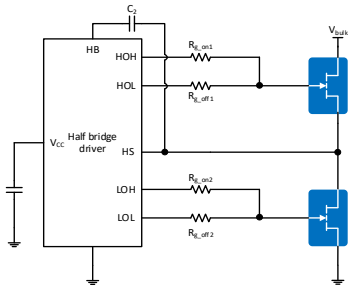
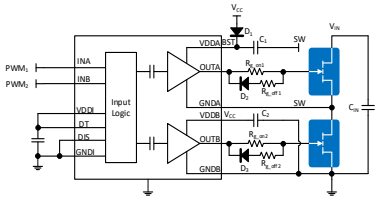
3、 Capacitances and speed: InnoGaN features smaller C_{ISS} and C_{RSS}, resulting in lower gate driving losses and faster switching speeds.

2. Gate driving circuit for InnoGaN

2.1. Categories of LV InnoGaN gate driving circuits

The categorization, features, and applications for InnoGaN gate driving circuits are summarized in **Table 2**.

Table 2 Categories of InnoGaN Driving Circuits

Categorization			Schematic	Specificities	Applications
Single	Non-isolated	Direct-driving		Simple driving circuits for high reliability and simpler driving loop design	Applications: Lidar、Low Power Modules Topologies：Flyback、single switch
Half-bridge	non-isolated	direct-driving		Simple driving circuit optimized specifically for GaN devices, high reliability and simpler driving loop design	Applications: power modules, in-car fast charger, notebooks , data center, MHEV, Class D, Topologies：Buck、Boost、Buck-Boost、full-bridge、half-bridge、LLC
	Isolated	Integrated digital isolators and drivers		Integrated with isolation and GaN driving, specifically optimized for driving with high reliability.	Field：Power Modules Topologies：full-bridge、half-bridge、LLC

2.2. Considerations for driver selection

When selecting a driver IC for LV InnoGaN products, these steps should be followed:

1. Verify Driving Voltage: Ensure the IC is compatible with 5V output voltage to meet the requirements of LV GaN products.

2. Voltage Tolerance and Compensation: Since the maximum gate voltage rating for LV InnoGaN is 6V and the recommended voltage is 5V, driving voltage stability is critical. It is generally recommended to use a driver IC with compensation and clamping to prevent performance degradation caused by insufficient driving voltage or device failure caused by overvoltage.

3. SW Pin Voltage Tolerance: The SW pin voltage tolerance must exceed the maximum possible reverse voltage V_{SD} during freewheeling. Or a Schottky diode is recommended in parallel with GaN to prevent IC failure caused by negative SW voltage.

3. Single-FET gate driving design

3.1. Direct-driving

3.1.1. Schematic of direct-driving circuit

The schematic of the direct-driving circuit is shown in **Figure 4**.

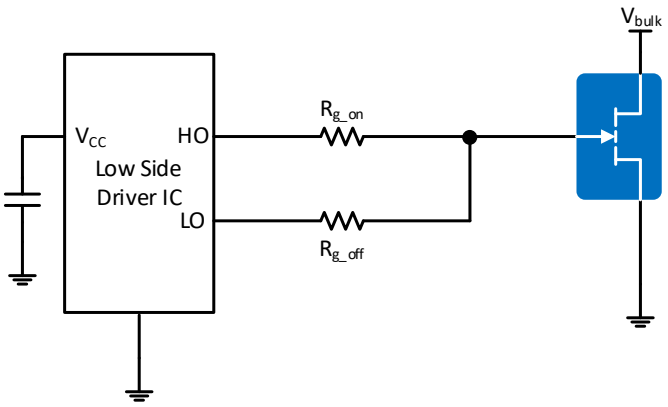


Figure 4 Direct-driving circuit

3.1.2. Functions of Key Components

The functions of the key components in the direct-driving circuit are listed in **Table 3**.

Table 3 Functions of key components in direct-driving circuit

Electronic component	Functions
R_{g_on}	Modify the turn-on speed of GaN FET
R_{g_off}	Modify the turn-off speed of GaN FET

3.1.3. Switching processes

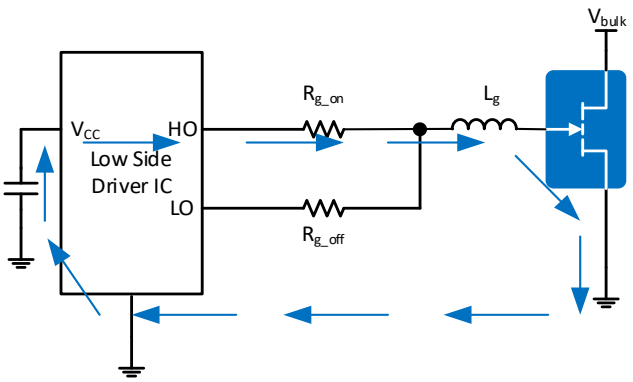


Figure 5 Turn-On loop of direct-driving circuit

During the turn-on process, the driving current loop is as shown in **Figure 5**. The current flows from the positive terminal of V_{CC} capacitor, through the driver IC, the gate resistor (R_{g_on}) and parasitic inductance (L_g) of the gate driving loop, then to the gate of the InnoGaN. The current returns to the negative terminal of V_{CC} capacitor from the source of the InnoGaN to the GND of driver IC.

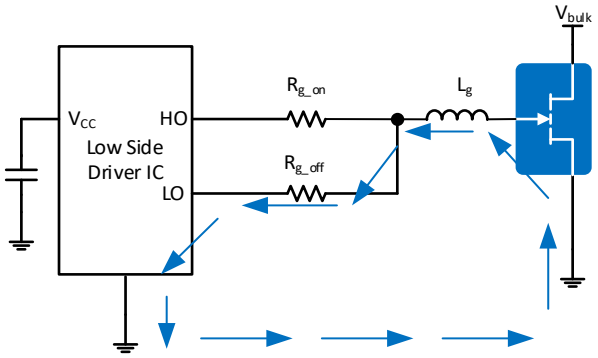


Figure 6 Turn-off loop of direct-driving circuit

During the turn-off process, the gate charge flows through L_g, R_{g_off}, and is rapidly discharged to GND inside the driver IC, as shown in **Figure 6**.

3.1.4. Design examples

Figure 7 and **Figure 8** show the schematic and layout design example of a direct-driving circuit design.

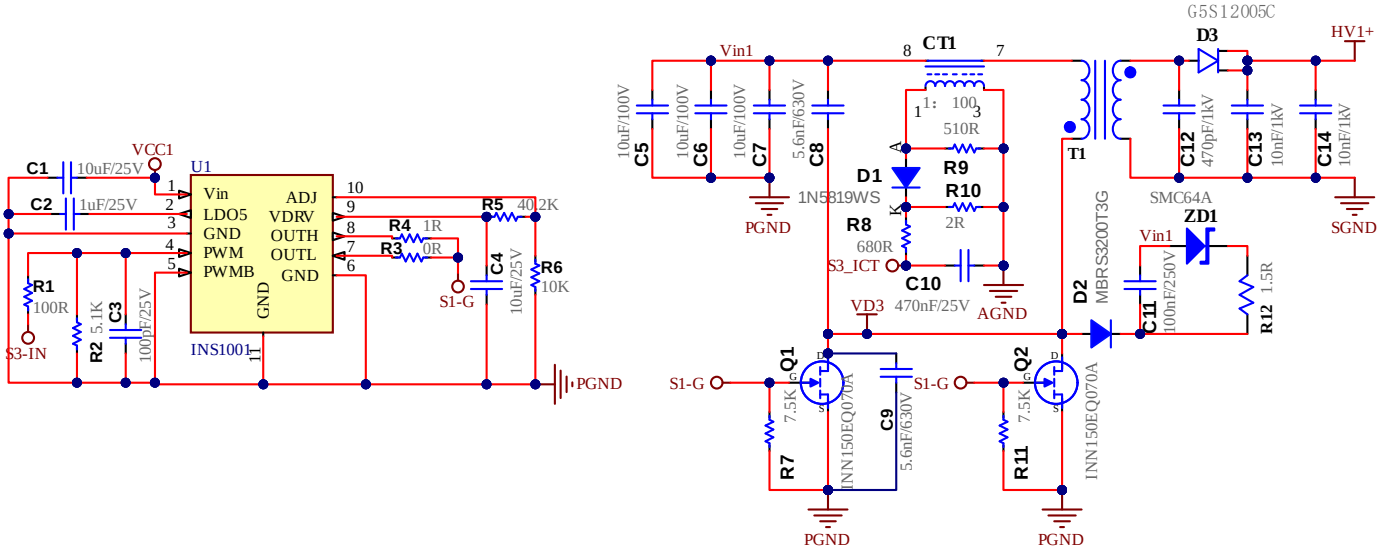


Figure 7 Schematic of direct-driving circuit design example

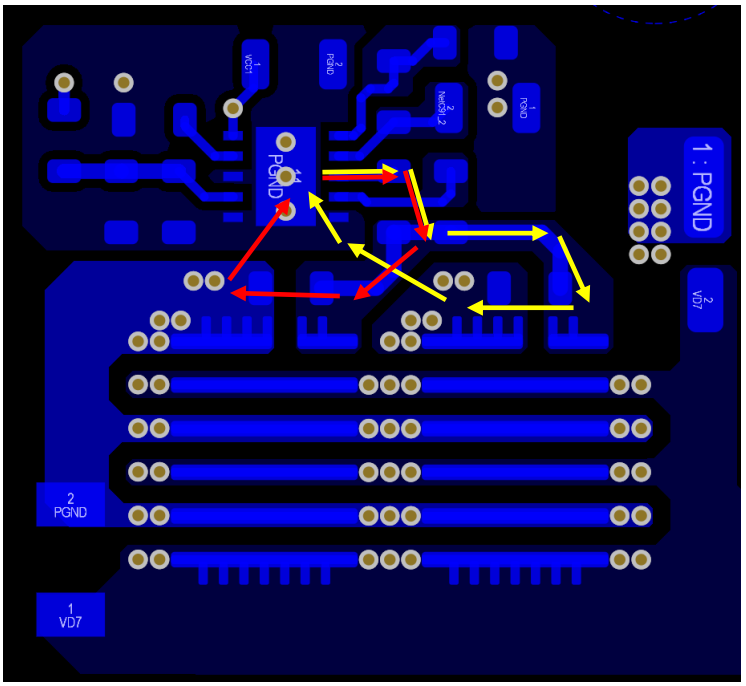


Figure 8 Layout of direct-driving circuit design example (The yellow and red arrows indicate the driving loops for two parallel switching devices.)

3.1.5. Design considerations

1、 Place the V_{CC} capacitor close to the driver IC pins to minimize the gate driving loop and reduce power supply oscillations.

2、 The driver should be positioned as close to the GaN device as possible to minimize parasitic inductance in the driving loop.

3、 Reduce coupling between the gate driving loop and the power loop to minimize common-source inductance.

For more layout design suggestions, refer to **AN006-InnoGaN Layout Design Guide**.

3.1.6. IC Recommendation

Several ICs suitable for direct-driving circuits are recommended in this section. Details such as part number, manufacturers, pull-up and pull-down resistances, propagation delay times, and application are listed in **Table 4**.

Table 4 Recommended ICs for Direct-Drive Circuit

Part Number	Manufacturer	Pulldown resistance/Pullup resistance（Ω）	Propagation Delay(ns)	Application
INS1001DE	Innoscience	1.3/0.5	35	Switch-Mode Power Supplies Boost, Flyback, and Forward Converters Half-Bridge and Full-Bridge Converters
LM5114	Texas Instruments	2/0.23	12	Universal single GaN low-side gate driver
LMG1020	Texas Instruments	-	2.5	GaN low-side gate driver for high-speed, high-frequency applications up to 60 MHz with a minimum pulse width of 1 ns
uP1964	uPI Semiconductor	2/0.5	30	Universal single GaN low-side gate driver

4. Half-bridge gate driving design

4.1. Non-isolated half-bridge gate driving

4.1.1. Schematic of non-isolated half-bridge gate driving circuit

Non-isolated half-bridge gate driving circuits are suitable for topologies such as LLC, synchronous Buck, and Boost. The block diagram is shown in **Figure 9**.

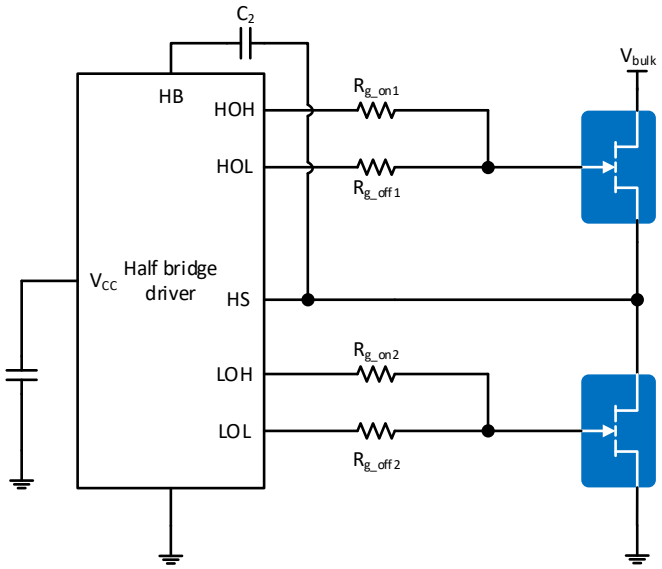


Figure 9 Non-isolated half-bridge gate driving circuit

4.1.2. Functions of Key Components

The functions of the key components in a non-isolated half-bridge gate driving circuit are listed in **Table 5**.

Table 5 Key components in non-isolated half-bridge gate driving circuit

Component	Functions
R_{g_on1} 、 R_{g_on2}	Modify turn-on speed of GaN FETs
R_{g_off1} 、 R_{g_off2}	Modify turn-off speed of GaN FETs

4.1.3. Switching Processes

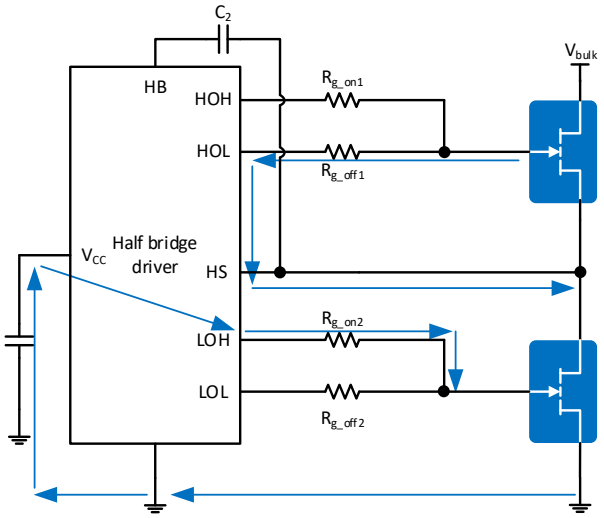


Figure 10 Turn-on loop of the low-side GaN and turn-off loop of the high-side GaN

Figure 10 shows the current loop during the low-side GaN turn-on and high-side GaN turn-off process

Low-side turn-on: Current flows from the positive terminal of the V_{CC} capacitor, through the IC's LOH pin and R_{g_on2} to the gate of the InnoGaN, and then returns to the negative terminal of the V_{CC} capacitor through the source of the InnoGaN.

High-side turn-off: When the half-bridge midpoint is low, the bootstrap capacitor (C_2) of the high-side is charged. Current flows from the gate through the IC's HOL pin and R_{g_off1}, pulling down to the high-side reference point (HS).

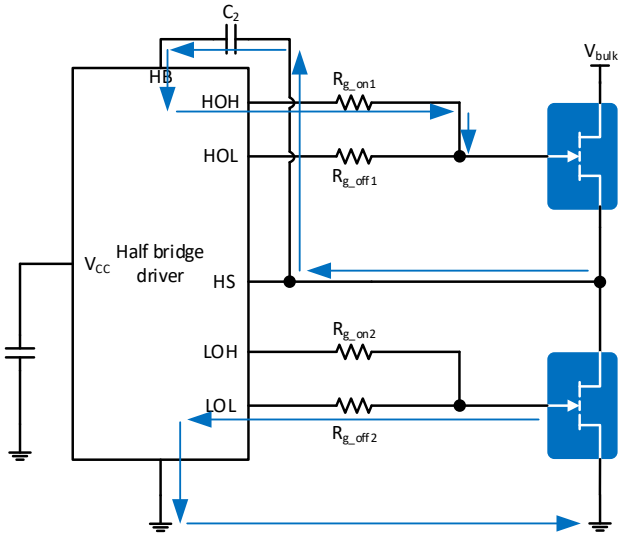


Figure 11 Turn-on process of the high-side GaN and turn-off process of the low-side GaN

Figure 11 shows the current loop during the high-side GaN turn-on and low-side GaN turn-off process

High-side turn-on: Current flows from the positive terminal of the high-side power supply capacitor, through the IC's HOH pin and R_{g_on1} to the gate of InnoGaN, and returns to the high-side reference point (HS) through the source of InnoGaN.

Low-side turn-off: Current flows from the gate through R_{g_off2} and the IC's LOL pin, pulling down to GND.

4.1.4. Design Examples

Figure 12 and **Figure 13** show the schematic and layout design example of the non-isolated half-bridge gate driving circuit.

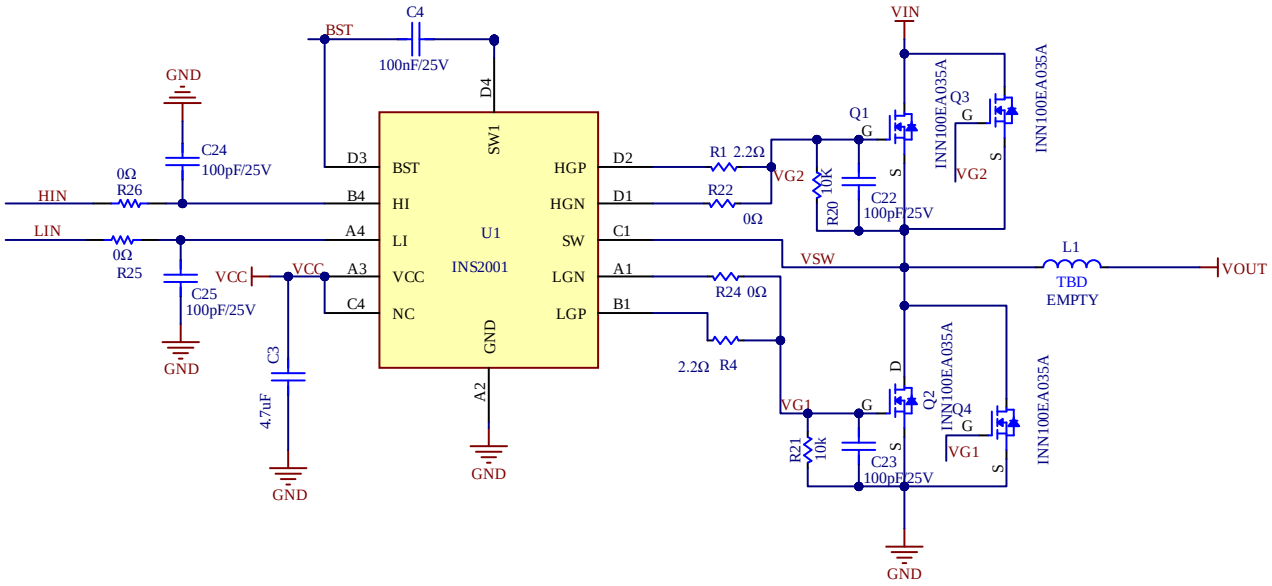


Figure 12 Example of non-isolated half-bridge driving circuit design

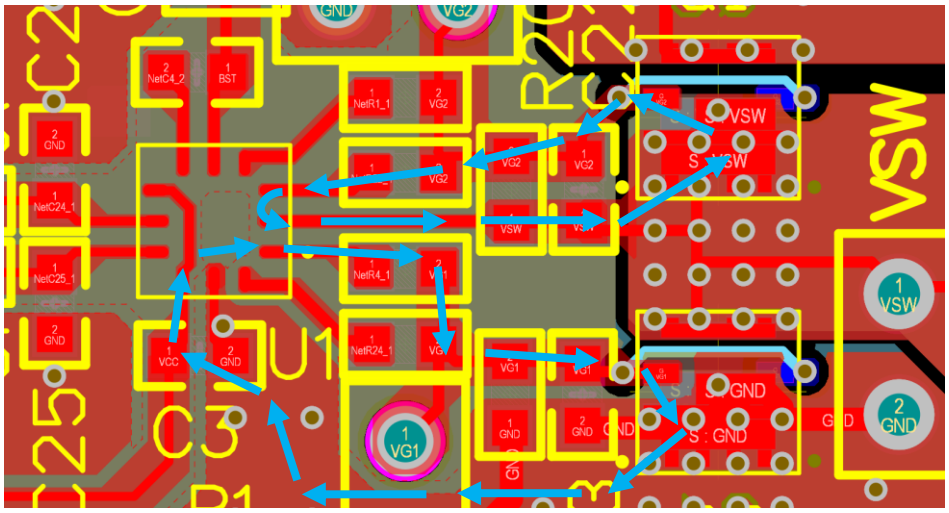


Figure 13 Example of non-isolated half-bridge layout design and current loop

4.1.5. Design considerations

1. Place the V_{CC} capacitor close to the driver IC pins to minimize the turn-on loop and reduce power supply oscillations.
2. Place the driver as close to GaN device as possible to reduce parasitic inductance in the gate driving loop.
3. Minimize coupling between driving loop and power loop to reduce common-source inductance.

Place the bootstrap capacitor near the driver IC pins, and separate the gate driving loop from the power loop to minimize the impact of power loop dv/dt on gate driving circuit.

4.1.6. IC Recommendation

Several control ICs suitable for non-isolated half-bridge circuits is recommended in this section. The information such as part number, manufacturers, maximum voltage ratings, propagation delay times, and application are listed in **Table 6**.

Table 6 Recommended control ICs for non-isolated half-bridge gate driving

Part Number	Manufacturer	Max voltage(V)	Propagation delay(ns)	Application
INS2001W INS2001FQ	Innoscience	100	14	48 V DC Motor Drive High Power Class-D Audio Power Amplifier Automotive 48 V/12 V Bi-directional DC-DC

INS2002W **INS2002FQ**	Innoscience	100	22	48 V DC Motor Drive High Power Class-D Audio Power Amplifier Automotive 48 V/12 V Bi-directional DC-DC
LMG1205	Texas Instruments	100	35	A universal GaN half-bridge driver that supports 100 V input
uP1966A	uPI Semiconductor	80	20	A universal GaN half-bridge driver that supports 100 V input
MPQ1918	MPS	100	20	High-side floating bias voltage rail operates up to 100 VDC

4.2. Isolated half-bridge gate driving

4.2.1. Schematic of isolated half-bridge gate driving circuit

In power supply applications requiring isolation, such as hard-switching full-bridge or phase-shift full-bridge topologies, isolation between the primary and secondary sides is necessary to meet system voltage withstand requirements. The application block diagram is shown in **Figure 14**.

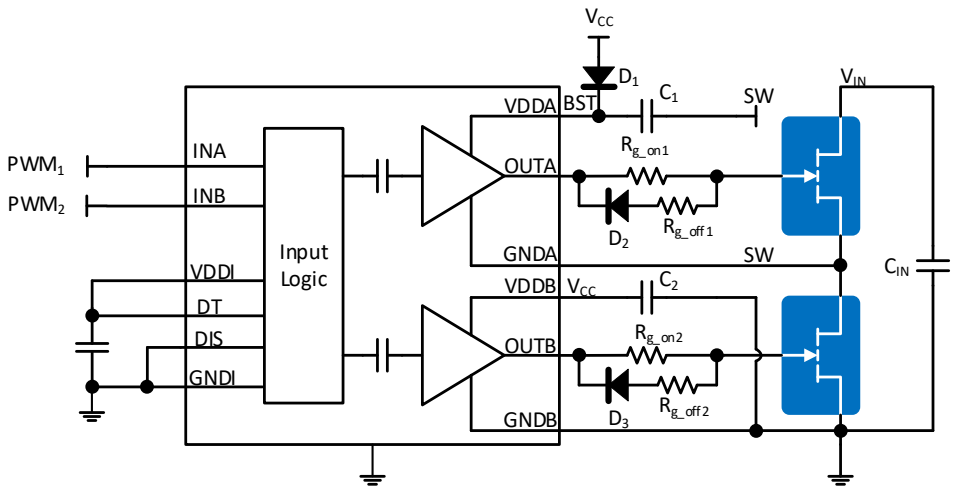


Figure 14 Isolated half-bridge gate driving circuit with integrated digital isolation

4.2.2. Switching processes

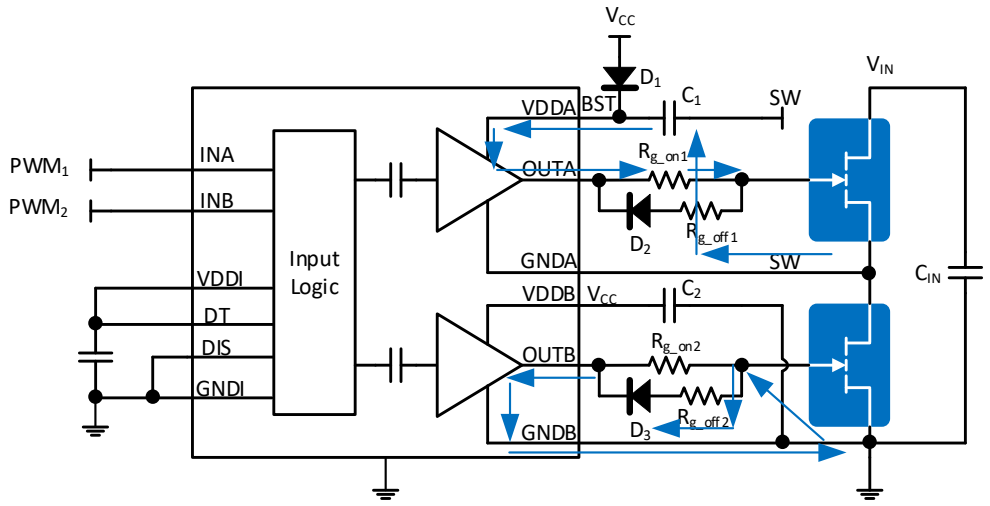


Figure 15 Turn-on process of high-side GaN and turn-off process of low-side GaN

Figure 15 shows the current loop during the high-side turn-on and low-side turn-off process.

High-side turn-on: Current flows from the high-side supply capacitor's positive terminal (VDDA), through the IC's OUTA pin and R_{g_on1} to the gate of InnoGaN. It returns to the high-side reference point (SW) through the source of InnoGaN.

Low-side turn-off: Current flows from the gate, through R_{g_off2} and diode D_3, to the IC's OUTB pin and is pulled down to GND.

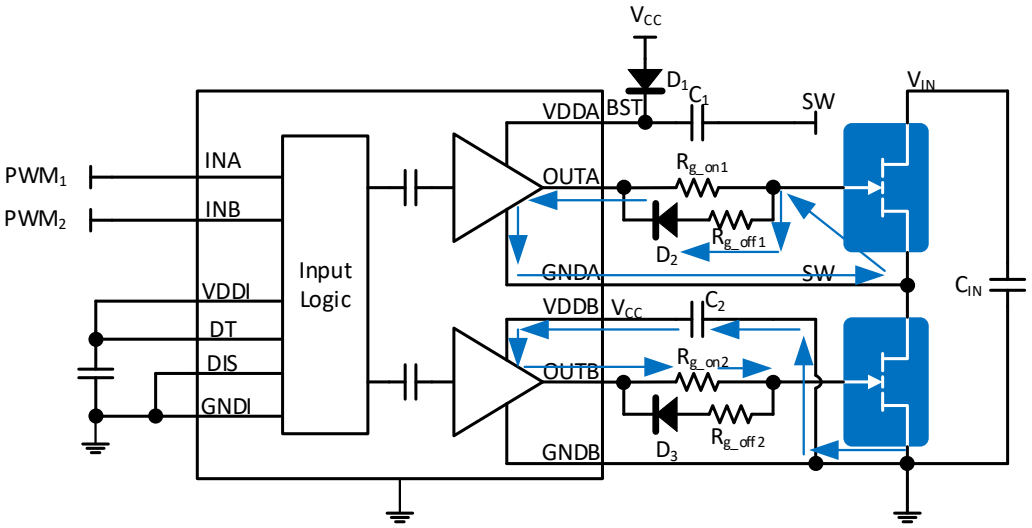


Figure 16 Turn-On Process of the Low-Side Device and Turn-Off Process of the High-Side Device

Figure 16 shows the current loop during the low-side turn-on and high-

side turn-off process.

Low-side turn-on: Current flows from the positive terminal (VDDB) of the low-side supply capacitor, through the IC's OUTB and R_{g_on2} to the gate of InnoGaN. It returns to the negative terminal of the capacitor through the source of InnoGaN.

High-side turn-off: When SW is low, the high-side bootstrap capacitor is charged. Current flows from the gate, through R_{g_off1} and diode D_2 to the IC's OUTA pin and is pulled down to the high-side reference point (SW).

4.2.3. Design examples

Figure 17 and **Figure 18** show the schematic and layout design examples of a isolated half-bridge gate driving circuit.

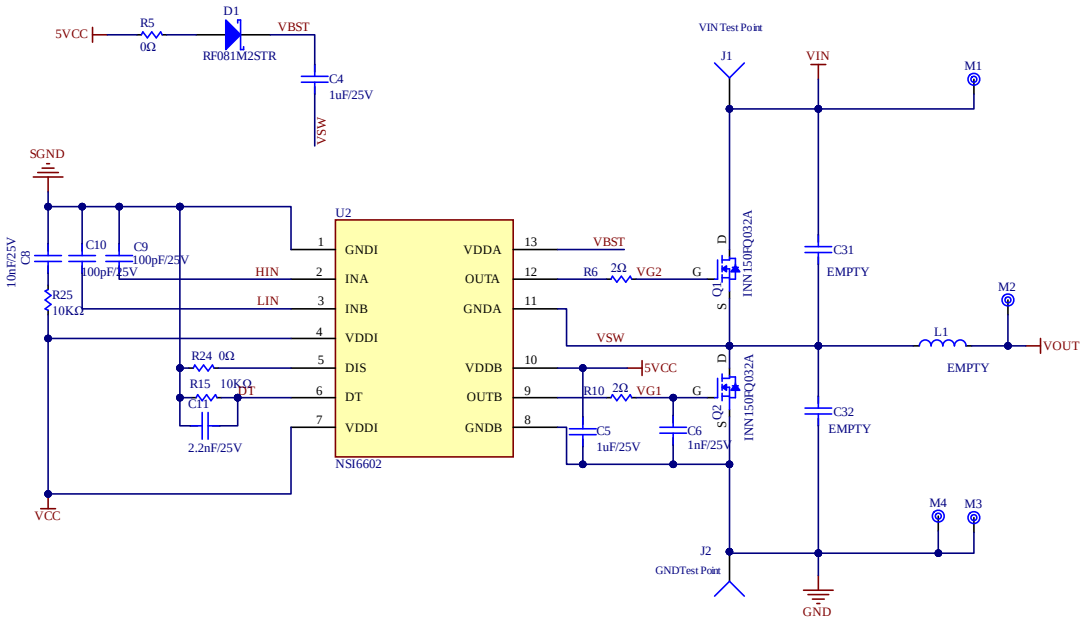


Figure 17 Example of isolated half-bridge driving circuit design

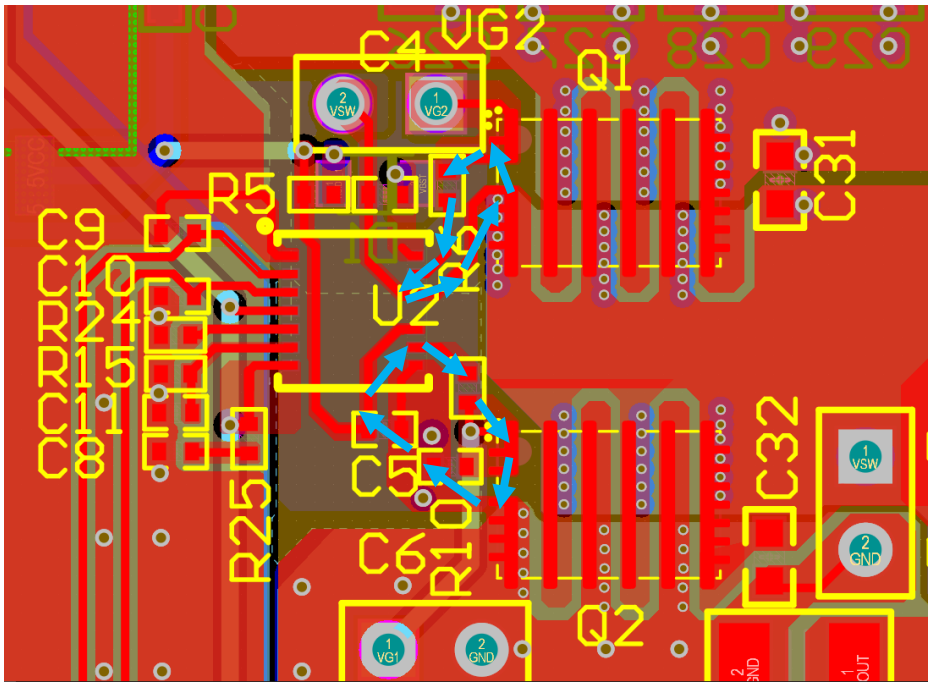


Figure 18 Example of isolated half-bridge layout design and current loop for low-side turn-on and high-side turn-off

4.2.4. Design considerations

1、Bypass capacitors: Use capacitors with low Equivalent Series Resistance (ESR) and low Equivalent Series Inductance (ESL) as bypass capacitors. Place them close to the power supply pins of the driver, such as VDDI-GND, VDDA-GNDA, and VDDB-GNDB.

2、 Placement of isolated drivers: Since high-frequency current charges and discharges the gate of the power transistors. Isolated driver should be placed close to the power transistors to minimize the gate driving loop area, improve EMI performance and mitigate ringing.

3、Reduce common-source inductance: Minimize common-source inductance to prevent adverse effects on switching performance due to high di/dt.

4.2.5. IC Recommendation

Several isolated half-bridge driving ICs are recommended in this section. The details such as part number, manufacturers, propagation delay times, and application are listed in **Table 7**.

Table 7 Recommended isolated half-bridge driving ICs

Part Number	Manufacturer	Propagation Delay(ns)	Application
NSI6602EA	Novosense	25	NSI6602E is a high reliability dual channel isolated gate driver which could be designed in variety switching power and motor drive topologies
Si8273	SILICON LABS	60	Si8273 controlled using the VIA and VIB input signals
Si8274	SILICON LABS	60	Si8274 controlled by a single PWM signal
UCC21550	Texas Instruments	33	UCC21550x-Q1 has a programmable dead time and a wide temperature range Isolation type dual channel gate driver series

Revision History

Date	Versions	Description	Author
2024/04/12	1.0	First edition	AE Team
2024/10/16	1.1	Update some of the content	AE Team
2025/02/07	1.2	Format correction, content update, and illustration update	AE Team

Note:
There is a dangerous voltage on the demo board, and exposure to high voltage may lead to safety problems such as injury or death.
Proper operating and safety procedures must be adhered to and used only for laboratory evaluation demonstrations and not directly to end-user equipment.

Reminder:
This product contains parts that are susceptible to electrostatic discharge (ESD). When using this product, be sure to follow antistatic procedures.

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